VALLIAMMAI ENGINEERING COLLEGE
Department of Information Technology

CS6303 COMPUTER ARCHITECTURE
Question Bank

Year :II year (2014-15) ODD SEMESTER

UNIT-1OVERVIEW AND INSTRUCTIONS

PART- A

1. What are the eight great ideas in computer architecture?
2. What are the five classic components of a computer?
3. What is the function of data path and control path?
4. What is instruction set Architecture?
5. Define application binary interface
6. Differentiate DRAM and SRAM.
7. Compare Volatile and nonvolatile memory.
8. List the advantages of Network Computer.
9. Define VLSI
10. Differentiate Throughput and Response Time
11. Write the CPU performance equation.
12. If computer A runs a program in 10 seconds, and computer B runs the same program in 15 seconds, how much faster is A over B.
13. What are the basic components of performance?
14. Write the formula for CPU execution time for a program
15. Write the formula for CPU clock cycles required for a program.
16. How will you measure the dynamic power dissipation?
17. Define – Stored Program Concepts
18. What are the fields in an MIPS instruction?
19. Write an example for immediate operand
20. Write operations to perform sum of four variables b,c,d,e and store the result in a.
21. List the advantages of multiprocessor over uniprocessor.
22. What are the different types ofoperands? Give examples
23. List the different addressing modes

PART-B
1. i)Discuss in detail about Eight great ideas of computer Architecture.(8)
   ii) Explain in detail about Technologies for Building Processors and Memory (8)
2. Explain the various components of computer System with neat diagram (16)
3. Discuss in detail the various measures of performance of a computer(16)
4. Define Addressing mode and explain the basic addressing modes with an example for each.
5. Explain operations and operands of computer Hardware in detail (16)
6. i)Discuss the Logical operations and control operations of computer (12)
   ii)Write short notes on Power wall(6)
7. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a.Which processor has the highest performance expressed in instructions per second?

b.If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

 c.We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

8. Assume a program requires the execution of 50×106 FP instructions,110×106 INT instructions, 80×106 L/S instructions, and 16×106 branchinstructions. The CPI for each type of instruction is 1, 1, 4 and 2 respectively.Assume that the processor has a 2 GHz clock rate.

a. By how much must we improve the CPI of FP instructions ifwe want the program to run two times faster?

b. By how much must we improve the CPI of L/S instructionsif we want the program to run two times faster?

c. By how much is the execution time of the program improvedif the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and

Branch is reduced by 30%?

9.Explain Branching operations with example

10.Explain the following addressing modes in detail with diagram

i)Immediate addressing ii)Register addressing, iii)Baseor displacement addressing, iv)PC-relative addressing v)Pseudodirect addressing

UNIT-II ARITHMETIC OPERATIONS
PART-A

1. Add 6_{10} to 7_{10} in binary and Subtract 610 from 710 in binary
2. Write the overflow conditions for addition and subtraction.
3. Draw the Multiplication hardware diagram
4. List the steps of multiplication algorithm
5. What is fast multiplication?
6. List the steps of division algorithm
7. What is scientific notation and normalization? Give an example
8. Give the representation of single precision floating point number
9. Define overflow and under flow with examples
10. Give the representation of double precision floating point number
11. What are the floating point instructions in MIPS?
12. What are the steps of floating point addition?
13. List the steps of floating point multiplication
14. Define – Guard and Round
15. Write the IEEE 754 floating point format.
16. What is meant by sub-word parallelism?
17. Multiply 100010 * 100110.
18. Divide 1,001,010ten by 1000ten.
19.Write the MIPS assembly code for the following C expression?
   $f = g + (h − 5)$
20.Write the corresponding C statements for the following MIPS assembly instructions
   add f, g, h
   add f, i, f

PART- B

1. Explain the Multiplication algorithm in detail with diagram and examples
2. Discuss in detail about division algorithm in detail with diagram and examples
3. Explain in detail about floating point addition with example
4. Explain in detail about floating point multiplication
5. Give the algorithm for multiplication of signed 2's complement numbers and illustrate with an example
6. Multiply the following pair of signed 2's complement numbers :
   $A = 010111$, $B = 101100$.
7. Add the numbers 0.5_{10} and -0.4375_{10} using binary Floating point Addition algorithm
8. Multiply $1.10_{10} \times 10^{10}$ and 9.200×10^{-5} using binary Floating point multiplication
9. Calculate the division of A and B
   $A : 3.264 \times 10^3$ $B: 6.52 \times 10^2$
10. Show the IEEE 754 binary representation of the number -0.75_{10} in single and double precision

UNIT III PROCESSOR AND CONTROL UNIT

PART-A

1. What is meant by data path element?
2. What is the use of PC register?
3. What is meant by register file?
4. What are the two state elements needed to store and access an instruction?
5. Draw the diagram of portion of datapath used for fetching instruction.
6. Define – Sign Extend
7. What is meant by branch target address?
8. Differentiate branch taken from branch not taken.
9. What is meant by delayed branch?
10. Write the instruction format for the jump instruction.
11. What are hazards? Write its types.
12. What is meant by forwarding?
13. What is pipeline stall?
14. What is meant by branch prediction?
15. What are the 5 pipeline stages?
16. What are exceptions and interrupts?
17. Define – Vectored Interrupts
18. What is meant by pipelining?
19. What are the five steps in MIPS instruction execution?
20. What are the three instruction classes and their instruction formats?
21. Write the formula for calculating time between instructions in a pipelined processor.

PART B

1. Explain the basic MIPS implementation of instruction set
2. Explain the basic MIPS implementation with necessary multiplexers and control lines
3. What are control hazards? Explain the methods for dealing with the control hazards.
4. Discuss the influence of pipelining in detail

5. Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall? What can be its resolution?
6. What is data hazard? How do you overcome it?What are its side effects?
7. Discuss the data and control path methods in pipelining
8. Explain dynamic branch prediction
9. How exceptions are handled in MIPS
10. Explain in detail about building a datapath
11. Explain in detail about control implementation scheme

UNIT IVPARALLELISAM

PART-A

1. What is meant by ILP?
2. What is multiple issue? Write any two approaches.
3. What is meant by speculation?
4. Define – Static Multiple Issue
5. Define – Issue Slots and Issue Packet
6. Define – VLIW
7. Define – Superscalar Processor
8. What is meant by loop unrolling?
9. What is meant by anti-dependence? How is it removed?
10. Differentiate in-order execution from out-of-order execution.
11. What is meant by hardware multithreading?
12. What are the two main approaches to hardware multithreading?
13. What is SMT?
14. Compare SMT from hardware multithreading.
15. What are the three multithreading options?
16. Define – SMP
17. Differentiate UMA from NUMA.
18. What is a multicore microprocessor?
19. What is a parallel processing program?
20. Define a cluster

PART- B
1. Explain Instruction level parallelism
2. Explain the difficulties faced by parallel processing programs
3. Explain shared memory multiprocessor
4. Explain in detail Flynn's classification of parallel hardware
5. Explain cluster and other Message passing Multiprocessor
6. Explain in detail hardware Multithreading
7. Explain SISD and MIMD
8. Explain SIMD and SPMD
9. Explain Multicore processors
10. Explain the different types of multithreading

UNIT V MEMORY AND I/O SYSTEM

PART-A

1. What are the temporal and spatial localities of references?
2. Write the structure of memory hierarchy
3. What are the various memory technologies?
4. Differentiate SRAM from DRAM.
5. What is flash memory?
6. Define − Rotational Latency
7. What is direct-mapped cache?
8. Consider a cache with 64 blocks and a block size of 16 bytes. To what block number does byte address 1200 map?
9. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address?
10. What are the writing strategies in cache memory?
11. What are the steps to be taken in an instruction cache miss?
12. Define – AMAT
13. What are the various block placement schemes in cache memory?
14. Define – MTTF and AFR
15. Define – Availability
16. What are the three ways to improve MTTF?
17. Define – TLB
18. What is meant by virtual memory?
19. Differentiate physical address from logical address.
20. What is meant by address mapping?

PART- B

1. Explain in detail about memory technologies

2. Explain in detail about memory Hierarchy with neat diagram

3. Describe the basic operations of cache in detail with diagram

4. Discuss the various mapping schemes used in cache design

   A byte addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block contains 132-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses – 200, 204, 208, 20C, 2F4, 2F0, 200, 204,218, 21C, 24C, 2F4. The pattern is repeated four times. Assuming that the cache is initially empty, show the contents of the cache at the end of each pass, and compute the hit rate for a direct mapped cache.

5. Discuss the methods used to measure and improve the performance of the cache.

6. Explain the virtual memory address translation and TLB withnecessary diagram.

7. Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals.

8. Explain in detail about interrupts with diagram

9. Describe in detail about programmedInput/output with neat diagram

10. Explain in detail about I/O processor.