Department of Computer Science & Engineering

QUESTION BANK

Subject: MPI **Faculty Name:Ch.Satish Kumar Reddy**
Branch: III CSE I Semester

UNIT-I

Questions (Theory type)

1. Distinguish between the terms microprocessor, microcomputer and micro controller. Write about the evolution of microprocessor.
2. Draw the architectural diagram of 8085 and explain the function of each block in detail.**April-09**

or

3. Give the brief overview of 8085 microprocessor
4. With a neat architectural diagram, explain the functioning of an 8086. **April-09**

or

Explain, why 8086 internal architecture is divided into BIU and EU? Discuss the A-bus, B-bus and C-bus and their use.**Nov/Dec-05**

5. Discuss briefly about pre-fetch queue in 8086.**April-08.**
6. Explain the function of following registers 8086 microprocessor. **April-09**
   a) AX,BX,CX,DX b) CS,DS,SS, ES c) BP,SP, SS, ES d) IP and instruction queue

or

Discuss the functions of all general purpose registers of 8086.Explain the special function of each register and instruction support for these functions.

7. What is memory segmentation ? Explain the use of segmentation in different applications. Explain how segmentation provides effective task switching mechanism.**Aug-07**

or

List out segmentation register of 8086. Explain how 8086 provides 1 MB memory address space using the segment registers. What is the purpose of extra segment.**August-06**.

8. Compare the flag registers of 8086 and 8085.**April-09**.
9. Write detail about the addressing modes of 8086 microprocessor.**April-09**.

Or

Describe the following addressing modes with some examples (i) Indexed addressing with displacement; (ii) I/O port addressing.**April-09.**

Or

Explain detail about the following addressing modes of 8086 with examples. ((i) I/O addressing (ii) Based indexed addressing with displacement.**April-09**

10. Explain the meaning of the following 8086 instructions, (i) Mov [3845h],bx (ii) add ax, [SI] (iii) Mov bx,2956h (iv) adc ax,bx (v) MUL (vi) IMUL (vii) DIV (viii) IDIV. **Aug-08,** . **April-09**.
11. Discuss the assembler directives with examples.**Aug-07,April-07**
12. Develop an assembly language program to multiply two BCD numbers of 2-digits each. **April-07**
13. Explain with an example, how a far procedure is declared as PUBLIC? Show how an external near procedure is called in main program?**Aug-07, April-07**

or

What is a procedure? Give an example to declare a procedure as near. Make this procedure as PUBLIC procedure. **Set 1 May11,Aug-07, April-07. April-09**

or

What are the different ways of passing parameters to and from procedures? Explain the methods with examples in assembly language.**Aug-07**.

14. Develop a PUBLIC procedure to convert 4-digi Hex to BCD number and return the value. **April-07**
15. Differentiae between procedures and macros using certain examples.**Aug-08, April-08**.

16. (a) Explain in detail the coding template for 8086 MOV instruction? (b) Write briey about i. PUBLIC directive ii. EXTERN directive **Set 2 May 11**
17. It is necessary to check the parity of the data byte in location 2000H:01FEH.If the parity is even store 00H otherwise store 0FFH in location 8000H:1000H. Give the instruction sequence for every addressing mode to achieve the above result. **Set 2 May 11**
18. (a) Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?
    (b) Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again.**Set 4 May 11**
19. 8086 processor do not provide memory indirect addressing mode. Show all possible ways to access a word from memory where the segment address is given in location C000H:1000H and the offset is given in location C000H:1002H. Give the instruction sequence for every addressing mode of 8086.?**Set 4 May 11, Set 2 Nov 10**
20. The register contents of 8086 is given below. CS=5000H, DS=8000H, SS=A000H, ES=B000H, SI=2000H, DI=6000H, BP=1002H, SP=0002H, AX=0000H, BX=5200H, CX=2000H, DX=2000H Calculate the effective address and physical address of the following instructions. (a) IMUL AX, [BP+BX-8D] (b) SBB AL, ES: SI+5D] (c) PUSH AX (d) AND AH, [SI+42D] (e) CMPSB (f) CMP DX, [SI] (g) XOR DH, [DI+8D] (h) DIV AX, [SI+2] **Set 1 May 11**
21. (a) What are the common flags in 8086 and 8085 processors? Discuss about each of the flags.
    (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment. **Set 3May 11**
22. (a) Explain memory addressing modes of 8086? Give an example for each addressing mode?
    (b) What is the purpose of Trap ag? Discuss how debugging feature is provided with the help of Trap flag in 8086? **Set 2 Nov 10**
23. (a) Draw the block diagram of 8086 and explain each block.
    (b) Discuss the addressing modes provided by 8086 and explain with examples. **Set 4 Nov 10**

UNIT – II

Questions (Program type)

1. Give the assembly language implementation of the following, (i) DO-WHILE (ii) FOR.**August-07**
2. Discuss various branch instructions of 8086 microprocessor, that are useful for relocation. **April-07,April-06, April-05**
3. What are the loop instructions of 8086? Explain the use of DF flag in the executin of string instructions. **Aug-06, Nov-05,May-04.**
4. Write an ALP in 8086 to move block of N bytes of data from source to destination. **April—09,Aug-08.**
5. Write an ALP in 8086 to add 5 bytes of data in an array by making use of procedure. **April-09,Aug—08.**
6. Write an ALP in 8086 to add two 16-bit hexa decimal numbers. **April-09,Aug—08**
7. Write an ALP in 8086 to find a maximum number in the array of 10 numbers. **April-09,Aug-08,April-08.**
8. Write a recursive program in 8086 ALP to find the sum f the first n-integers. **April-09,Aug-08,April-08.**
9. Write a program in 8086 to ad two 8-bytes of data available in memory location array1 and array2. Store the result in aray3. **April-09**
10. Write an ALP to count number of 0s in a 16 bit binary string. **April-09**
11. Write an ALP in 8086 to add two 16 digit packed BCD numbers. **April-09,April-08**
12. Write an ALP in 8086 to divide a 32-bit number by a 16-bit number. **April-09, April-08.**
13. Write an ALP in 8086 to sort a given set of 8-bit unsign integers into ascending order b bubble sort method. **Aug-08.**
14. Write an ALP in 8086 to display the string “WELCOME” on the screen. **Aug-08**
15. Write an ALP in 8086 to count number of positive and negative numbers from an array of 8-bit integers. **Aug-08, April-08**
16. Write an ALP in 8086 to exchange a block of N bytes of data between source and destination. **Aug-08,April-08.**
17. Using REPEAT-UNTIL construct, develop a sequence of 8086 instructions that reads a character string from the keybard and after pressing the enter key the character string is to be displayed again.
    Aug-07, April-07,Set 1 May 11
18. Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again.
    April-07, April-05
19. Develop an 8086 assembly language program that will determine if a given sub string is present or not in a main string of characters. Place the result as P if present else place N in memory location result **Aug-07**

20. Develop an 8086 assembly language program that reads a key from the keyboard and converts it to uppercase before displaying it. The program needs to terminate on typing the 'Crtl + C' key combination.**Set 3May 11**
21. (a) Using REPEAT-UNTIL construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again.
    (b) What is a procedure? Give an example to declare a procedure as near? Make this procedure as PUBLIC procedure? **Set 2 Nov 10**
22. (a) Using DF ag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions.

(b) Discuss how procedures are defined and involved in assembly language programming.**Set 4 Nov 10**

23. (a) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N,where N is a two-digit Hex number?

(b) Give the assembly language implementation of the following.i. REPEAT – UNTI **Set 1 Nov 10** ii. FOR

UNIT-III

Questions(Theory type)

1. Describe the function of the following pins and their use in 8086 based system. (i)NMI (ii) LOCK (iii) TEST (iv) RESET (v) TEST (vi) RQ/GT_0 and RQ/GT_1 (vii) QS0 and QS1 (viii) s0, s1, s2 **Nov-05, April-05**
2. What are the control signals useful for inter-processor communication using 8086? What instruction set support is provided in 8086. **Aug-07, Nov-05**
3. What is the purpose of ALE, BHE, DT/R and DEN pins of 8086? Show their timing in the system bus cycle of 8086. **Aug-07, April-07**
4. With appropriate pin diagrams explain the minimum and maximum mode operations of 8086. **April-09.**

   or

   With a neat pin diagram explain the maximum mode operation of 8086. **April-09**

   Or

   Show the circuit required to generate the upper and lower I/O strobes in minimum and maximum modes of operation of 8086. **Aug-07,April-07.**
5. What is the minimum number of bus cycles that can occur between the time an interrupt request is recognized and the first instruction in the interrupt routine is fetched ? **Aug-08,Aug-07,April-07**
6. Distinguish between a memory read and write machine cycle. Draw the timing diagrams in minimum and maximum modes f operation.
7. What is function of ready pin in 8086? Draw the circuit diagram for wait state generation between 0 and 7 wait states and draw the corresponding timing diagram **April-06,Aug-06.**
8. Explain briefly about memory interfacing with 8086 microprocessor. **April-09,Aug-08**.
9. Explain how static RAM are interfaced to 8086. Give necessary interface diagram assuming appropriate signals and memory size. **Aug-08,April-08.**

   Or

   With the help of basic cell explain SRAM and DRAM . discuss the advantages of the memories. **April-07, Nov-05, April-05**.

   Or

   Differentiate between static and dynamic RAMs give some example. **April -09**.
10. With neat sketch explain the internal organization of SRAM chip. List out the input and output pins Discuss their function in a system. **Aug-07**.
11. With a neat sketch explain the function of memory array of PROM **April-07, Aug-06, Aug-06.**

    or

    `Draw the basic cell structure of EPROM and explain the principle of operation. **April-07, Aug-06**.

    Or

    Distinguish between EPROM and E2PROM. Mention their application areas. **Aug-07, April-07.**
12. Why 8086 memory is mapped into 2 byte wise banks? What logic levels are fond with BHE and A0 when 8086 reads a word from the address 0A0A H? **Aug-07.**
13. Explain the need for DMA in microprocessor based systems. **April-09.**

    or

14. With a neat block diagram, explain the working of 8257controller. **April-09, Aug-08.**

    or

15. Explain need of DMA. Discuss in detail about DMA transfer method. **Aug-08,April-08.**

    or

    With a neat block diagram explain the working of 8237 DMA controller **April-09, Aug-07, April-06**.

or

Explain demand transfer mode and block transfer mod of 8237. **Aug-07, April-07**.

or

Show how 8237's are cascaded to provide more number of DRQ's and explain the operation.**Aug-07,April-07.**

16. Explain how memory to memory transfer is performed with 8237. **Aug-07,April-07**.
17. Discuss the following signal descriptions? (a) ALE=PROG (b) EA / VPP (c) PSEN (d) RXD (e) INT0 / INT1 (f) TXD (g) T0 AND T1 (h) RD **Set 2 May 11**
18. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait status and draw the corresponding timing diagram. **Set 4 May 11,Set 1 Nov 10**
19. (a) What is the difference between HALT state and HOLD state? Discuss the status of different control pins of 8086 in both the states?

(b) What are the control signals useful for inter processor communication using 8086? What instruction set support is provided in 8086? **Set 1 May 11**

20. With detailed hardware and the associated algorithm, explain how a real time clock will be implemented in an 8086 based system. **Set 1 May 11**
21. Explain the following data transfer schemes. (a) Programmed I/O (b) Interrupted I/O (c) DMA **Set 3 May 11**
22. Describe the function of the following pins in 8086 maximum mode of operation. (a) MN/ MX (b) RQ/GT0 and RQ/GT1 (c) QS0 & QS1 (d) LOCK **Set 2 Nov 10**

UNIT-IV

Questions(Theory type)

1. Draw the block diagram of 8255 and explain each block. **April-07**

or

Describe the three modes of operations for 8255 using relevant diagrams. **Aug-08**

or

Distinguish between a system clock and peripheral clock and explain briefly the control block of 8255 **April-09**

Or

Explain mode 1 input operation and mode 1 output operation in 8255 with examples.**Aug-08**

or

What is meant by Interfacing ? Explain the brief description of PPI **Aug-08**

or

What is BSR mode of operation? How it is useful in controlling the interrupt initiated data transfer for mod1 and mode2 ?**Aug-08, April-07, Aug-06**

or

Distinguish between mode set control word and BSR control word f 8255. **April-09,Aug-08,April-08**

or

Discuss about the following control words of 8255. (i) Mode set control word (ii) Bit set/reset control word. **April-09**

2. Describe the operation of 8279 with a neat block diagram.
3. Explain about interfacing of a DAC with 8086 using 8255 **April- 09**

Explain how an ADC can be interfaced to a microprocessor. Give the required instruction sequence to acquire one sample from ADC. **April-09**

4. (a) Draw the block diagram of 8279 and explain each block?

(b) Explain different modes of operation of 8255 and how they are initialized in control word? **Set 2 May 11**

5. (a) Draw the block diagram of 8279 and explain the functionality?

(b) Design a counter type ADC using 8255? Make necessary assumptions and give the software listing?**Set 4 May 11**

6. Interface a stepper motor with 8-step input sequence to 8086 based system and write the instruction sequence to move the stepper motor 20 steps in clockwise and 12 steps in anti-clockwise direction.**Set 1 May 11**
7. (a) 8255 is interfaced with 8086 processor with the address map of 8000H to 8003H. Give the hardware design (b) Port A is con_gured in mode 2 with active interrupt. Give the instruction sequence for initialization? Provide the timing diagram of the handshake signals for the bi-directional data transfer? **Set 3 May 11**
8. **(**a) Explain the application of stepper motor in microcomputers?

(b) Explain with a neat block diagram the working of dual slope ADC? How do you interface the dual slope ADC to microprocessor? Give the required instruction sequence to acquire one sample from ADC?S**et 2 Nov10**

Questions (Program type)

9. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations. (i) Port A as input and ports B and C as output in ode 0 operation. (ii) Port A in mode 1 operation and port B in mode 0 operation **Aug-08**
10. Supose that the beginning address of an 8255 is 0900H and write a program sequence that wil, (i) Put bot groups A and B in mode 0 with orts A and C being input ports and port B as an output port. (ii) Put group A in mode 1 with port A being an input and PC6 and PC7 being outputs and group B in mod 1 with ort B being an input.**April-08**
11. Write the BSR control word to set bit 3 of port C and also write the BSR control word to reset bit 3 of port C. Introduce a 1 msec delay between set and reset of bit 3 of port C. **April-08**
12. Explain the transistor buffer circuit used to drive 7 segment LEDs **April-07, Aug-06**
13. Interface a stepper motor to the 8086 microprocessor system and write an 8086 assembly language program to control the stepper motor.
14. Write an ALP in8086 to generate a symmetrical square wave form with 1 kHz frequency. Gie the necessary circuit setup with a DAC. **April-09,Aug08, April-08**
15. Interface a 12-bit DAC to 8255 with an address map of 0C00H to 0C03H. the DAC provides output in the rang of +5V to -5V write the instruction sequence. (a) For generating a square wave with a peak to eak voltage of 4 V and the frequency will be selected from memory location 'F' (b) For generating a triangular wave with a maximum voltage of +3 and a minimum of 2V . **Aug-07,April-06,Nov-05,April-05.**
16. It is necessary to initialize interrupt for mode 2 operation of port-A and mode1 operation of port-B with the 8255 address map of 0600H to 0603H. Give the complete hard ware design to interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A and Port B to mode 1? **Set 4 Nov 10**
17. Interface two 8255s to 8051 with starting address of 0FFF0H? Show the hardware design? Write the instruction sequence to initialize all ports of 8255s as input ports in mode 0 **Set 4 Nov 10**
18. Interface an 8-bit DAC to 8255 with an address map of 0804H to 0807H. The DAC provides output in the range of +5V to - 5V. Write the instruction sequence for the following?

(a) For generating a square wave with a peak to peak voltage of 2V and the frequency will be selected from memory location 'FREQ'.

(b) For generating a triangular wave with a maximum voltage of +4V and a minimum of -2V. **Set 1 Nov 10**

UNIT-V

Questions(Theory type):

1. Describe the interrupt vector table of Intel processors. **April-08**
2. Give the priority of 8086 interrupts, hardware and software. Explain why single step interrupt is having lower priority.**Aug-07**
3. Discuss the sequence of operations performed in the interrupt acknowledge cycle. Aug-07
4. What is the difference between maskable and non-maskable interrupts. Give some examples. **Apr-09, Aug-08**
5. Discuss the following i) single step execution ii) Interrupt on overflow.**April-08**
6. Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt. **Aug-07**
7. What is type-2 interrupt? Explain the condition for initiating type-2 interrupt? What is the priority of this interrupt in 8086? Discuss about DOS and Bios interrupts. Give necessary examples.**April-08**
8. **8259** PIC architecture and interfacing, cascading of interrupt controller and its importance. **Aug-07**
9. Differentiate between initialization command words and operation command words of 8259. **April-09.**
10. Describe some important features of 8259 interrupt controller. **April-09**
11. Explain the following terms with reference to 8259. i) END of interrupt ii) Automatic rotation iii) poll command iv) Read register command. **April-06, May-08**
12. Explain the importance of 8259 interrupt controller and explain how does it handle the interrupt. **April-08**
13. How many initialization command words are required for a single 8259 in an 8086 based system? Explain their format. **April-08**
14. Distinguish between master and slave mode operation of 8259. **April-09**
15. Give an interfacing diagram, which shows the connections between 8086 and 8259. **April-08**
16. Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority? **Set 2 May 11**
17. It is necessary to serve 15 interrupt requests using 8259's. The address map for the 8259's is given from 0100H to 0103H. Show the complete interface with 8086 system bus? These 15 interrupts are to be requested from

interrupt type 060H on words, with level trigged mode and auto end of interrupt. Give the initialization sequence for all 8259's. **Set 2 May 11**

18. Write an initialization sequence for an 8259 that is the only 8259 in an 8086 based system, with an even address of 0040H that will cause. (a) Request to the level triggered mode (b) IR0 request to an interrupt type 28 (c) SP/EN to output a disable signal to the data-bus transceivers. (d) The ISR bits to be cleared automatically at the end of second INTA pulse. (e) The IMR to be cleared. (f) The highest priority interrupt will be IR3. **Set 4 May 11**
19. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0C00H, to be IR5, IR6, IR7, IR0, IR1, IR2, IR3, IR4. Solve this problem when the current priority is IR1 and for the second time assuming the current priority to be IR7?

(b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? **Set 3 May 11**

20. In an 8086 based system it is necessary to serve 64 IRQs from di_erent initiators.The allocated address space for 8259s is from 0700h to 070FH. Give the complete design by choosing the appropriate address locations in the above range? Give the initialization sequence for all 8259's with each IRQ activated in level triggered mode and the starting interrupt is type 40H? **Set 2 Nov 10**
21. Why do we prefer interrupt driven data transfer than programmed I/O transfer? Show the complete hardware design to resolve the multiple interrupts based on priority **Set 4 Nov 10**
22. (a) Explain DOS interrupt 21H and its functions?

(b) Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 interrupt? S**et 4 Nov 10**

23. (a) Explain initialization command words and their sequence of operation?

(b) Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 interrupt? **Set 1 Nov 10**

24. Discuss the following signal descriptions? (a) ALE=PROG (b) EA / VPP (c) PSEN (d) RXD (e) INT0 /INT1 (f) TXD (g) T0 AND T1 (h) RD **Set 1 Nov 10**

UNIT-VI

Questions(Theory type)

1. Discuss the types of serial communication.**April -09**

or

Distinguish between synchronous and asynchronous serial data transmission techniques. Discuss the advantages and disadvantages. **April-07, April-09**

2. Discuss the data transmission standards and their specifications. **Aug-08**
3. Draw the flow chart showing how synchronous serial data can be sent from a port line using software routine. **Aug-06**
4. A terminal is transmitting asynchronous serial data at 2400bd. What is the bit time? Assuming 7 data bits, a parity bit and 1 stop bit how long does it take to transmit one character?**April-05**
5. Draw the block diagram of 8251 and explain abut each block. **Aug-08, April-05**

Or

What are the important features of 8251? **May-08**

6. Give the status register of 8251 and explain each bit. **April-08**
7. Explain the following control words of 8251 with suitable examples, i) Mode word ii) Command word. **May-08**
8. Explain the interfacing of 8251 with 8086 with necessary circuit diagram. **April-09**
9. Explain about the three errors in asynchronous serial transmission. **Sep-08**
10. Write the instruction sequence to re-initialize the above 8251 in synchronous mode with even parity, single SYNC character and 8-bit character size.**May-06**
11. What is the difference between 20mA current loop and RS232-C standard. **Aug-07**
12. Give the specifications of RS-232C. **May-08, May-06**
13. Draw the circuit of RS-232 to TTL conversion and explain this interface. **Sep-08**
14. Draw the circuit of TTL to RS232 and explain the necessity of this interface. **Aug-07**
15. Explain about line driver and line receiver used in serial communication . **May-08**
16. (a) Explain USB operation?

(b) Interface 8251 with 8086 at address 0A010H. Initialize it in asynchronous mode, with 6 bit character size, baud rate factor 16, one start bit, two stop bits, odd parity enable? **Set 2 May 11, Set 2 Nov 10**

17. (a) Write a sequence of instructions to communicate to a modem using 8251 at address 080H. **Set 4May11**
18. Give the specifications of i. RS-232C **Set 4 May 11** ii. RS-423A **Set 1 Nov 10**

19. (a) Discuss the serial data transmission standards and their specifications.
(b) Explain the necessity of RS232 to TTL interface and draw the circuit.
(c) Draw the circuit of TTL to RS232 and explain the necessity of this interface.**Set 1 May 11**
20. (a) What are the MODEM control lines? Explain the function of each line?Discuss how MODEM is controlled using these lines with necessary sequence of instructions?
(b) Interface 8251 with 8086 at address 0F0H. Initialize it in asynchronous mode,with 8 bit character size, baud rate factor 16, one start bit, two stop bits, even parity enable? **Set 3 May 11**
21. (a) How do we connect RS-232C equipment i. To data terminal type devices? ii. To serial port of SDK 86, RS-232C connection? **Set 1 Nov 10**

UNIT-VII

1. Explain the basic differences between a microprocessor and a microcontroller. **April-09**
2. Enrich salient features of 8051 family of microcontrollers. **April-07,April-06**
3. Draw the architectural diagram of 8051 microcontroller and explain in detail about each block. **April-09**
4. Discuss about various addressing modes of 8051. **Aug-08**
5. Discuss in detail about parallel I/O ports in 8051 microcontroller. Also explain how these ports are accessible for specific applications. **April-09**

UNIT-VIII

1. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller.
   i) PCON ii) PSW iii) IP iv) TMOD. v)TCON vi)SCON **Aug-07,Nov 10,May 11**
2. Discuss the register set of MCS-51 family of microcontrollers. **Nov-05**
3. Draw and discuss the formats and bit definitions of TCON SFR in 8051 microcontroller. **Nov-05**
4. Explain with waveforms, the different modes of counter/timer in 8051.**April-09**
5. Explain the interrupt structure of 8051.**Aug-08**
6. Discuss in detail about memory and I/O interfacing of 8051. **Aug-08**
7. How does 8051 differentiate between the external and internal program memory? **Sep-07**
8. Interface 8255 I/O ports with 8051. The address of port A should be 0000h.**Aug-08**
9. (a) Explain the instruction support of 8051 to read data from lookup tables stored in EPROM?
(b) Explain the counter/timer operation of 8051? Explain how this can provide clock for baud rate setting in serial data transmission through 8051? **Set 4 May 11**
10. An 8051 based system requires external memory of four 4Kbytes of SRAM each and two chips of EPROM of size 2Kbytes. The EPROM starts at address 2000H. SRAM address map follows EPROM map. Give the complete memory interface.**Set 1May 11**
11. (a) Discuss the following signal descriptions? i. INT0/INT1 ii. TXD iii. T0 AND T1 iv. RD