SEMBODAI RUKMANI VARATHARAJAN ENGINEERING COLLEGE

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

Sub.Code : CS2202 Semester : III

Sub.Title : DIGITAL PRINCIPLES AND SYSTEM DESIGN

UNIT-1
BOOLEAN ALGEBRA AND LOGIC GATES
PART – A(2marks)

1. What is meant by Digital Systems?
2. What is meant by Decimal Systems?
3. What is meant by Duality Theorem?
4. Convert the number (111111) binary to decimal?
5. Convert the number (83) octal to Decimal?
6. Convert the number (34891) Decimal to octal?
7. Convert the number (6725) octal to binary?
8. Convert the number (1011010101) binary to octal ?
9. Convert the number (4608) decimal to Hexadecimal ?
10. Convert ABC Binary to Hexadecimal ?
11. Define Gray Code?
12. Prove that x + x = x?
13. Define Associative Law and Distributive law?
14. Define Boolean algebra?
15. Define Boolean Function?
16. Define Min terms?
17. Define Max terms?
18. List out the Logic gates?
19. Draw the Symbol of And gate and OR gate?
20. Draw the neither Symbol of NOR, NAND and NOT gate?
21. Draw the Symbol of Exclusive OR gate?
22. Write the Truth Table of And gate?
23. Write the Truth Table of Exclusive OR gate?
24. Define Demorgan's Theorem?
25. Define Karnaugh Map?
26. List out the types of K-Map?

PART – B

1. a. Explain the various types of K-Map with Examples (12)
b. Prove that x + 1 = 1 (2)
c. Prove that x + xy = x (2)
2. a. Express the Complement of the Following function in sum of Midterms and product of Maxterms F(A,B,C,D) = B'D+A'D + BD (10)
b. Express the Complement of the following function in sum of Midterms F(A,B,C,D) = Σ (0,2,6,11,13,14) (6)
3. a. Simply the Boolean Function Using Three Variable K-Map F(X, Y, Z) = Σ (3, 4, 6, 7) (8)
b. Simply the Boolean Function Using Four Variable K-Maps F(W,X,Y,Z) = Σ (0,1,2,4,5,6,8,9,12,13,14) (8)

4. a. Explain logic operations with NAND Gates? (8)
b. Explain Multilevel NAND Gates? (8)
5. a. Explain Implementation of NOR Gates ? (8)
b. Explain AND- OR Invert Implementation (8)
6. a. Explain BCD Code with Examples (6)
b. Explain Excess 3 Code with Examples? (6)
c. Convert the number (28) Decimal to Excess 3 Code (4)
7. a. List out the Procedure for converting Binary to Gray Code (4)
b. Convert the number (1011) binary to gray? (4)
c. Explain 7 - Bit ASCII Code ? (8)

UNIT –II
COMBINATIONAL LOGIC
PART – A(2marks)

1. What is meant by Combination Circuits?
2. Draw the Block Diagram of Combination circuit?
3. What is meant by Half – Adder?
4. What is meant by Half – Subtractor?
5. What is meant by Full – Adder?
6. What is meant by Full – Subtractor?
7. What are Universal Gates?
8. Explain the Hardware Description Language?
9. What are the methods are available in HDL?
10. What is meant by Netlist?
11. What is Difference between Simulation and simulator?
12. What is Synthesis tool?
13. What is meant by VHDL Language?
14. What is meant by Verilog HDL?
15. What are elements of Verilog HDL?
16. What is Test Bench?

PART – B

1. a. Explain the Design procedure for Combination Logic Circuits (6)
b. Explain the Logic implementation of half–adder and half-subtractor (10)
2. a. Explain Logical Implementation of Full – adder and Full – Subtractor (10)
b. Draw the Logic Diagram for BCD to Excess 3 code Converter with Explain (6)
3. a. Explain the analysis procedure for combinational circuit (6)
b. Explain the 4- bit Full adder (4)
c. Explain the Block Diagram of BCD Adder (6)
4. a. Explain the 4 – Bit Magnitude Comparator (10)
b. Explain the Design Procedure for HDL (6)
5. a. What is meant by model and modeling ? (5)
b. Explain the Hardware Simulation (5)
c. Explain Hardware Synthesis (6)
6. a. Explain the Binary to BCD Convertor (10)
b. Explain the Binary Parallel adder (6)
7. a. Explain the excess 3 to BCD Code Converter (10)
b. Explain the Binary Adder- Subtractor (6)

UNIT – III
DESIGN WITH MSI DEVICES

PART – A(2 marks)

1. What is meant by Decoder and Encoder?
2. What is meant by Multiplexer and Demultiplexer?
3. Draw the Logic Diagram of 4:1 mux
4. Draw the Logic Diagram of 1:4 Demux
5. What is meant by ROM?
6. What are the three types of PLD?
7. What are the types of ROM?
8. Explain PROM?
9. Explain EPROM ?
10. Explain EEPROM ?

PART- B

1. a. Explain the Logic Diagram of 3 to 8 line Decoder (8)
b. How to Construct the 4 x 16 Decoder with two 3 x 8 Decoder (8)
2. a. Explain the 4 to 1 line Multiplexer (8)
b. Explain the 2 to 1 line Multiplexer (8)
3 a. Explain the Programmable Logic array (8)
b. Explain the Programmable array Logic (8)
4. a. Comparison between PROM, PLA and PAL (6)
b. Realise the function gives using a PLA with 6 Input, 4 Outputs and 10 AND (10) Gates

$F1(A,B,C,D,E,F) = \Sigma m(0,1,7,8,9,10,11,15,19,23,27,31,32,33,35,39,40,41,47,63)$

$F2(A,B,C,D,E,F) = \Sigma m(8,9,10,11,12,14,21,25,27,40,41,42,43,44,46,57,59)$

5. a. Write a behavioral for 4:1 MUX using Verilog HDL (8)
b. Write a behavioral model for 1:4 DeMux using Verilog HDL (8)
6. a. Write a structural model for 4:1 Mux and 1:4 DeMux using Verilog HDL (16)

UNIT – IV

SYNCHRONOUS SEQUENTIAL LOGIC

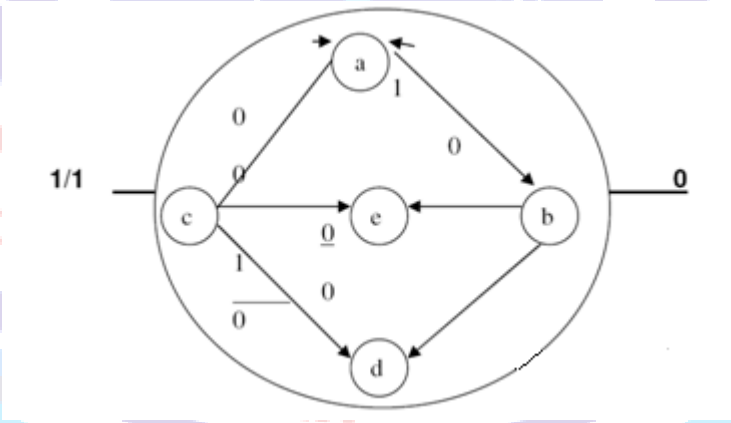
PART – A(2 marks)

1. What is meant by sequential circuit?
2. Draw the Block Diagram of sequential circuit?
3. What is Flip Flop?
4. What are the types of Flip Flop?
5. What is meant by Race around condition?
6. What is meant by Edge Triggered Flip Flop?
7. What is meant by Set up time?
8. What is meant by hold time?
9. What is meant by propagation delay?
10. What are categories of propagation delay?
11. Define Tplh?
12. Define Tphl ?
13. Draw the Cross coupled inverters ?
14. What is meant by Shift Register with types ?
15. What is difference between Moore and Mealy Circuit Model?
16. What is state diagram?
17. Draw the state diagram for Mealy and Moore Circuit?
18. What is meant by state equation?
19. What is meant by state reduction ?

20. What is meant by state assignment ?
21. What is meant by counter ?
22. What are the types of counter ?

PART – B

1. a. Write the verilog code generate for paralled load up / down counter (8)
b. Write a verilog code for D Flip Flop and R-S Flip Flop (8)
2. Explain R-S Flip Flop and Clocked R-S Flip Flop (16)
3 .a. Explain S-R Flip Flop (8)
b. Explain D Flip Flop (8)
4. a. Explain JK Flip Flop (11)
b. Explain T Flip Flop (5)
5. a. Explain Master Slave Flip Flop (8)
b. Explain the Edge Triggered Flip Flop (8)
6. a. Convert it JK Flip Flop in to T Flip Flop (8)
b. Convert it JK Flip Flop in to D Flip Flop (8)
7. a. Convert it D Flip Flop in to T Flip Flop (8)
b. Convert it T Flip Flop in to D Flip Flop (8)
8. a. Explain Serial in Serial out Shift Register (8)
b. Explain Serial in parallel out Shift Register (8)
9. a. Explain parallel in parallel out Shift Register (8)
b. Explain parallel in Serial out Shift Register (8)
10. Design sequential circuit for a state diagram? (16)



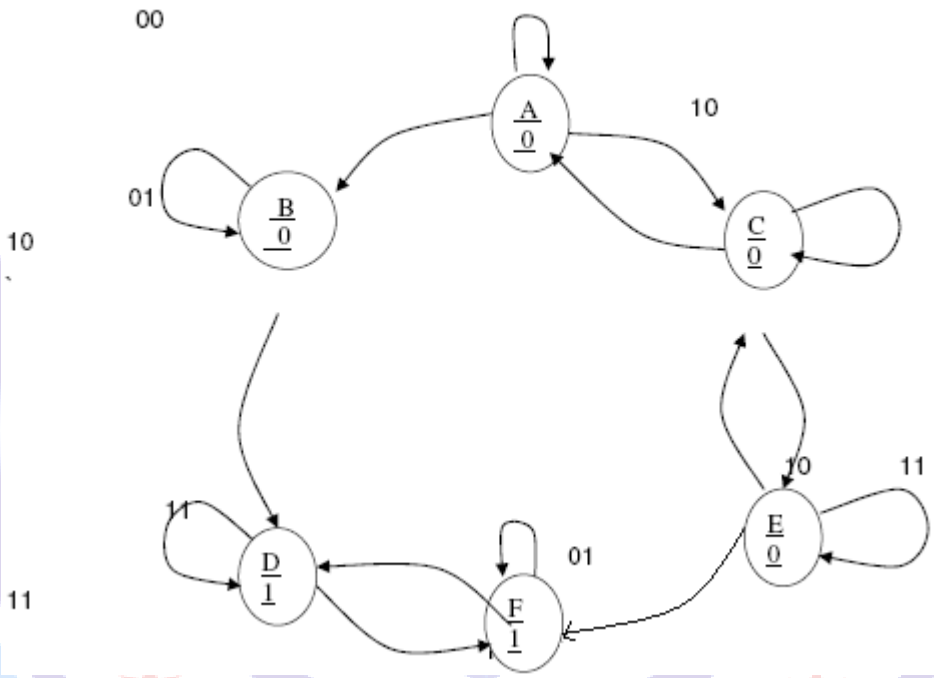
UNIT V
ASYNCHRONOUS SEQUENTIAL LOGIC
PART A(2marks)

1. What is difference between Synchronous sequential circuit and Asynchronous sequential Circuit?
2. What is meant by secondary variable and Excitation variables?
3. Draw a block diagram of Asynchronous Sequential circuits?
4. What is meant by Races?
5. What is meant by Cycle?
6. What are two techniques are available in critical race Free State assignment?
7. Draw the transition diagram with race free state assignment?

8. What is one hot state assignment?

PART – B

1. a. Explain the one hot state assignement (8)
b. Explain the shared – Row state assignment (8)
2. Design an asynchronous sequential circuit that has two input x2 , x1 and one output 2 when x1 = 0 the output 2 is 0. The first change in x2that occur while X1 is 1 will cause output 2 to be1. The output 2 will remain 1 until x1 returns to 0? (16)



3. Explain the classification of Race- Free State Algorithm? (16)
4. a. Explain the Hazards in combinational circuits? (6)
b. Explain the Hazards in sequential circuits? (10)