Code No: 07A80305 **R07** **Set No. 2**

IV B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
Common to Mechanical Engineering, Automobile Engineering
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What is the function of a Multiprocessor system and list out the various characteristics of Multiprocessors?
   (b) Explain how the Multiprocessors are classified based on their memory organization. [10+6]
2. (a) What is implied mode, immediate mode, register mode, register indirect mode, auto increment and auto decrement mode.
   (b) What is Zero address instruction, one address instruction? [8+8]
3. (a) With a neat diagram, discuss in detail about the possible address assignment for a byte-addressable 32-bit computer.
   (b) Draw the block diagram showing various connections of the main memory to the CPU. Also, explain about issues related to their bus structures. [7+9]
4. A computer uses a memory unit with 256K words of 32bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, register code part to specify one of 64 registers, and an address part.
   (a) Draw the instruction word format and indicate the number of bits in each part.
   (b) How many bits are there in data and address inputs of memory? [16]
5. (a) What is the function of a FIFO buffer?
   (b) Draw the complete circuit diagram of 4 × 4 FIFO buffer and explain it in detail. [1+15]
6. (a) What is the difference between microprocessor and micro program? Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessors?
   (b) Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory? [8+8]
7. Represent decimal number 7777 in:
   (a) BCD
   (b) excess - 3 code

(c) 2421 code. [16]

8. (a) How do you determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.

(b) Mathematically, show that the theoretical maximum speedup that a pipeline can provide is 'K', where 'K' is the number of segments in the pipeline.[6+10]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A80305 **R07** **Set No. 4**

IV B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
Common to Mechanical Engineering, Automobile Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Explain the significance of RISC system. Does RISC support. Complex instruction set computer concepts and operations. [16]

2. Explain with block diagram the typical functional blocks of a computer system, and explain the computer types with respect to the functional blocks. [16]

3. (a) Consider a single-transistor dynamic memory cell. Assume that C = 50 fento-farads and the leakage current through the transistor is about 9 pico amperes. The voltage across the capacitor when it is fully charged is equal to 4.5V. The cell must be refreshed before this voltage drops below 3V. Estimate the minimum refresh rate.
   (b) Discuss in detail about various features of ROM, PROM and EPROM.[6+10]

4. (a) With a neat block diagram, explain about one possible way of seperating the execution unit into eight functional units operating in parallel.
   (b) Bringout atleast two differences between (i) SSID & SIMD (ii) MISD & MIMD.[8+8]

5. Using a 4bit counter with parallel load and 4 bit address, draw a block diagram that shows how to implement the following statements and explain:

   x: R1<- R1 + R2 //Add R2 to R1
   x y : R1<- R1 +1. // Increment R1 [16]

6. (a) With a neat block diagram explain the various processes involved in system bus structure for multi processors.
   (b) What is the function of a cross bar switch network and how many switch points are there in a cross bar switch network that connects 'P' processors to 'm' memory modules? [10+6]

7. A computer has 16 registers an ALU, with 32 operations and a shifter with eight operations, all connected to a common bus system

   Show the bits of the control word that specify the micro operation R4 < - R5 + R6. [16]

8. (a) Draw the truth table of a four-input priority encoder and explain it in detail.
   (b) Design a parallel priority interrupt hardware for a system with eight interrupt sources. [6+10]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A80305 **R07** **Set No. 1**

IV B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
Common to Mechanical Engineering, Automobile Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are the functions of an array processor?
   (b) Differentiate between Attached and SIMD Array Processors with respect to any six parameters.
   (c) Compare Vector and Array Processings. [4+6+6]
2. What are basic computer registers, how are they effected when memory operations are done? [16]
3. What is RISC? How does this differ from other computer, explain? [16]
4. (a) What is Symbolic micro program, explain?
   (b) Taking an example design a control unit. [8+8]
5. (a) Bringout the differences between the shared and distributed memory multi-procesors.
   (b) Discuss how the Multiprocessor organization will improve the system performance. [8+8]
6. Draw the necessary diagrams and explain the following in detail:
   (a) Source-initiated transfer using handshaking.
   (b) Destination-initiated transfer using handshaking. [8+8]
7. A 1024 × 1024 away of 32- bit numbers is to be "normalized" as fikkiws. For each column, the largest element is found and all elements of the column are divided by this maximum value. Assume that each page in the virtual memory consists of 4K bytes, and that 1M bytes of the main memory are allocated for storing data during this computation. Suppose that it takes 40 ms to load a page from the disk in to the main memory when a page fault occurs.
   (a) How many page faults would occur if the elements of the array are stored in column order in the virtual memory?
   (b) How many page faults would occur if the elements are stored in row order?
   (c) Estimate the total time needed to perform this normalization for both arrangements a and b. [5+5+6]
8. Derive the circuits for a 3-bit parity generator and 4bit parity checker using an even parity bit. [16]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: 07A80305 **R07** **Set No. 3**

IV B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
Common to Mechanical Engineering, Automobile Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are symbolic micro program and binary micro program?
   (b) What is the importance of arithmetic logic shift unit in design of control unit? [8+8]
2. (a) 'Parallel Processing can be viewed from various levels of complexity'. Explain the statement with necessary reasons.
   (b) List out and explain various advantages of a parallel processing system.[6+10]
3. (a) Draw the diagrams of frame format and control field format in bit-oriented protocol and explain about it in detail.
   (b) What is the minimum number of bits that a frame must have in the bit-oriented protocol? [13+3]
4. (a) What is an interrupt, explain different interrupts in a computer system?
   (b) What is STACK? How is stack organized in memory? [8+8]
5. What is 4 bit adder subtractor? A 4 bit adder subtractor has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs: S3, S2, S1, S0 and C4: [16]

M	A	B
0	0111	0110
0	1000	1001
1	1100	1000
1	0101	1010
1	0000	0001

6. (a) Describe in detail about Associative-mapped cache with necessary diagrams.
   (b) A blockset associative cache consists of a total of 64 blocks divided in to four-block sets. The main memory contains 4096 blocks, each consisting of 128 words:
      i. How many bits are these in a main memory address?
      ii. How many bits are there in each of the TAG, SET and WORD fields? [12+2+2]
7. (a) Bringout the differences between the cross bar switch and multistage switching networks.

Code No: 07A80305 **R07** **Set No. 3**

(b) Construct a diagram for a 4 × 4 omega switching network. Show the switch setting required to connect input 3 to output 1. [8+8]

8. A 36bit floating point binary number has eight bits plus sign for the exponent and 26 bits plus sign for the mantissa. The mantissa is a normalized fraction. Numbers in mantissa and exponent are in signed magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero? [16]

⋆ ⋆ ⋆ ⋆ ⋆