PSG POLYTECHNIC COLLEGE, COIMBATORE - 641 004

G12303 DIGITAL LOGIC DESIGN

Model Question Paper

Time: 3 Hours **Max.Marks: 100**

Instructions:

1. **Group A** and **Group B** questions should be answered in the Main Answer book.
2. Answer any **TEN** questions in **Group A**. Each question carries three marks.
3. Answer **ALL** questions either **(a)** subdivision or **(b)** subdivision in **Group B**. Each question carries 14 marks.

Group – A **Marks: 10 x 3 = 30**

1. Write the advantages in operating as digital mode
2. Convert the following numbers into its decimal equivalent: (i) $(314)_8$ (ii) $(1011\ 1100)_2$
3. Perform the following division in binary; 11011 / 101
4. Construct the two basic gates using universal gates.
5. State and its prove deMorgan's theorem
6. Simplify the Boolean expressions to a minimum number of literals: xyz'+ x'yz+x'yz'.
7. Draw the block diagram of 4X1 multiplexer and write its truth table.
8. Using k-map, find the simplified Boolean equation for the given values.
   F(a,b,c,d)=Σ(3,4,5,7,9,13,14,15)
9. Design a half adder and simplify using K-map.
10. Define level triggering and edge triggering.
11. Show the characteristics equation for the complement output of JK flip flop is Q'(t+1)=J'Q'+KQ'.
12. Draw the logic diagram of 4 bit SIPO shift register
13. Give the number of bytes stored in the memories listed below: (i) 8K*16 (ii) 2T*8
14. Compare the EPROM & Flash Memory
15. Draw the internal organization diagram of a 64X4 RAM

Group– B **Marks: 5 x 11 = 55**

16. a) (i) Convert the following binary numbers to hexadecimal & to binary (5)
    (1) 1.10010 (2) 110.010
    (ii) How many printing characters are there in ASCII? How many of them are special characters. (9)

    (OR)

    b) (i) Perform the subtraction on the given unsigned binary numbers using the 2's complement (5)
    (1) 10011-10001 (2) 100010-100011
    (ii) Represent the decimal number 5137 in (1) BCD (2) Gray code (3) ASCII (9)
17. a) (i) Express the Boolean function F=A+B'C as a sum of minterms. (5)

(ii) Find the complements of expression (1) (x'+y+z')(x+y') (9)

(OR)

b) With the circuit diagram, explain the principle of operation 2 input TTL NAND gate.

18. a) Construct a 16*1 multiplexer with two 8*1 and one 2*1 multiplexers.

(OR)

b) Implement full adder with a decoder & NAND gates.
The adder inputs are A, B, C & D and the outputs are S & Co.

19. a) Construct a JK flip flop , using a D-Flip flop, a 2-1 line multiplexer, and an inverter.

(OR)

b) What is the difference between serial & parallel transfer? Which transfer method is the fastest one? Explain how to convert serial data to parallel.

20. a) Draw a PLA circuit to implement the following functions:
i) F1= A'B+AC'+A'BC' ii) F2=(AC+AB+BC)'

(OR)

b) Explain in detail about the RAM.