### **MODEL QUESTION PAPER**

TED(15)-3042

(REVISION-2015)

Reg No.....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING / TECHNOLOGY

## **DIGITAL ELECTRONICS**

Time:3 hours

(Maximum Marks: 100)

## **PART-A**

(Maximum marks : 10)

I.Answer the following questions in one or two sentences. Each question carries 2 marks.

1.Write radix of a binary number system.

2.List any two weighted codes.

3. Define fan in of a logic gate.

4. List the applications of shift register.

5. Define accuracy of Digital to Analog Converter.

#### **PART-B**

(Maximum marks : 30)

II. Answer any five of the following questions. Each question carries 6 marks.

1. Describe BCD code and EXCESS 3 code .

2. Draw and explain TTL inverter.

3. Design a full subtractor.

4. Differentiate between synchronous and asynchronous logic circuits.

5.Draw and explain a serial in parallel out shift register.

6. Draw and explain a 3 bit up counter using JK flip flop.

7. Draw and explain the working of R-2R type Digital to analog converter.

### **PART-C**

(Maximum marks : 60)

Answer one Full question from e ach unit. Each question carries 15 marks.

## UNIT-1

III a. Convert the following decimal numbers to binary and hexa decimal.

1.(32.82) <sub>10</sub>	2.	(638.53) <sub>10</sub>	
3.( 423.05) <sub>10</sub>	4.	(93.53) <sub>10</sub>	(8 marks)

b. Implement basic gate using NAND gate only.

(7 marks)

(5\*6=30)

Marks

(5\*2=10)

Signature.....

IV a.Subtract using 2's complement 1. (320) <sub>10</sub> –(250) <sub>10</sub>	t method. 2.( 435) <sub>10</sub> –(625) <sub>10</sub>	(8 marks)		
b. Simplify the given expression Y=Σ (1,5,6,1213,14	using Karnaugh map. )+d(2,4)	(7 marks)		
UNIT-2				
V.a. Draw and explain CMOS NAN	Digate .	(8 marks)		
b. Describe the operation of 4:1	multiplexer with circuit diagram.	(7 marks)		
	OR			
<ul><li>VI. a. Define the terms related to T</li><li>1. noise margin</li><li>2. Propaga</li><li>3. fan out</li><li>4. VOH</li></ul>	TL logic gates. tion delay	(8 marks)		
b. Draw and explain 3 bit enco	der.	(7 marks)		
UNIT-3				
VII. a. Discuss JK flip flop with truth	table using NAND gates.	(8 marks)		
b. Explain the working of ring of	counter with truth table.	(7 marks )		
OR				
VIII. a. Discuss various types of shif	t registers.	(15 marks)		
	UNIT-4			
IX. a. Draw and explain a mod-10 r	pple counter using JK flip flop.	(8 marks )		
b. Draw and explain the working	g of R-2R type Digital to analog converter.	(7 marks)		
OR				
X. a. Differentiate synchronous and	asynchronous counters.	(8 marks)		
b.Explain weighted resistor type	e Digital to Analog converter with suitable	e circuit diagram . (7 marks)		

# OR