A4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein.** **(1x10)**

1.1   Von Neumann architecture of computer is mainly characterized by
A)   Separate storage and signal path ways for their instructions and data
B)   Stored- program concept emphasizing storing of data as well as the instructions to manipulate that data, in the same way
C)   Swiftly execution of program
D)   None of the above

1.2   A refinement of SR flip-flop in which indeterminate condition of the SR type is defined as
A)   JK Flip-flop
B)   D Flip-flop
C)   T Flip-flop
D)   None of the above

1.3   1000 1111 is representation of -15 in
A)   In Signed - 1's complement representation
B)   In Signed - magnitude representation
C)   In Signed - 2's complement representation
D)   None of the above

1.4   With R1 = 1010, and R2 = 1100, the output of logic microoperation statement
         P : R1 ← R1⊖ R2 with P = 1 and ⊖ representing exclusive OR microoperation is
A)   1110
B)   1000
C)   0110
D)   None of the above

1.5   The address of memory word containing the address of the operand in instruction code is called
A)   Indirect address
B)   Immediate address
C)   Direct address
D)   None of the above

1.6   Which of the following expression is in Polish notation?
A)   A * B + C * D
B)   + * A B * C D
C)   A B * C D * +
D)   None of the above

1.7   For numbers in Sign-magnitude notation, the addition of magnitude of both numbers is performed if the result of XOR of sign digits of both numbers is
A)   Zero
B)   One
C)   Zero or one
D)   None of the above

1.8   Suppose each transmitted character consists of 11 bits and is being transmitted at the rate of 11 characters per second in serial transmission. The transfer rate is
A)   100 baud
B)   110 baud
C)   121 baud
D)   None of the above

1.9   Memory used for backup is called
A)   Virtual memory
B)   Main memory
C)   Auxiliary memory
D)   None of the above

1.10   Extra segment register in 8086 assembly language is
A)   A spare segment registers
B)   Used for referring data in some string manipulation instruction
C)   Used for referring program code
D)   None of the above

2.   Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" answer sheet supplied with the question paper, following instructions therein.   (1x10)

2.1   Every logical gates of computer handle multiple inputs.
2.2   Multiplexer is also called data selector.
2.3   Overflow condition is never generated on addition of a positive number and a negative number.
2.4   Four logic microoperations AND, OR, XOR and Complement are sufficient to implement all 16 microoperations.
2.5   BSA (Branch and Save Return Address) instruction can be performed in one clock cycle.
2.6   IP is used to push or pop items into or from the stack.
2.7   Subtraction is implemented by taking numbers in 1's complement.
2.8   In DMA, CPU merely delays its memory access operations.
2.9   Address space is allowed to be smaller than memory space in computer with virtual memory.
2.10   Effective address of an operand in Assembly refers to the distance of data from the beginning of a segment.

3. **Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein.** **(1x10)**

	X		Y
3.1	Multi-input gate sensitive to logic 0 on any one of its inputs, irrespective of any value at other inputs.	**A.**	Normalized
3.2	Storage element employed in clocked sequential circuit.	**B.**	Associative memory
3.3	A floating point number with non-zero most significant digit of mantissa.	**C.**	AND
3.4	A digital circuit which forms arithmetic sum of two bits and a previous carry.	**D.**	Non-vectored interrupt
3.5	Second part of an instruction code containing operand.	**E.**	Immediate instruction
3.6	Converting expression to evaluate arithmetic expression in stack computer.	**F.**	Full adder
3.7	Multiplication of two numbers in 2's complement form.	**G.**	Post fix
3.8	In interrupt-Initiated I/O, branch address is assigned to a fixed location in memory.	**H.**	In fix
3.9	Memory unit access by content.	**I.**	NOT
3.10	Reversing (changing ones to zeroes and vice versa) the bits of operand in Assembly language.	**J.**	Restoring method
		K.	Flip-flop
		L.	Booths algorithm
		M.	Vectored interrupt

4. **Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein.** **(1x10)**

A.	Pipelining	**B.**	END	**C.**	XOR
D.	Detecting	**E.**	Software	**F.**	
G.	Hit ratio	**H.**	EEPROM	**I.**	ADD
J.	Binary adder	**K.**	Instruction Register	**L.**	Hardware
M.	Program Counter				

4.1 Complement of AND is _____.

4.2 Flash memory is a form of _____.

4.3 A digital circuit which generates the arithmetic sum of two binary numbers of any length is called _____.

4.4 Parity bit is error _____code.

4.5 The address of the next instruction to be executed is available in _____.

4.6 A _____interrupt is initiated by executing an instruction.

4.7 In implementing hardware algorithm for addition and subtraction of two numbers in sign-magnitude notation, the sign bits of two numbers are compared through _____ gate.

4.8 _____is a technique of decomposing a sequential process into sub-operations with each sub-process being executed in special dedicated segment which operates concurrently with all other segments.

4.9 The performance of cache memory is measured by _____.

4.10 _____ is assembler directive.

PART TWO
(Answer any **FOUR** questions)

5.

a) What is full adder? Give its truth table and express simplified Boolean function of full adder as sum of product form. Draw the logic diagram using NAND gate.

b) Explain how floating point representation of number is done? When do you say the floating point number is normalized? Represent the number $(+52.25)_{10}$ as floating point binary number with 32 bits. The normalized fraction mantissa has 24 bits and exponent has 8 bits.

(8+7)

6.

a) Draw 4-bit adder–subtractor circuit and explain how does it work? Explain 4-bit combinational circuit incrementer through diagram and explain how it can be extended to an n-bit binary incrementer.

b) A digital computer has a common bus system for the registers of 32 bit each. The bus is constructed with multiplexers.
   - i) How many selection inputs are there in each multiplexer?
   - ii) What size of multiplexors are needed?
   - iii) How many multiplexors are there in bus?

(10+5)

7.

a) How is the program executed in the computer? Write all phases of each instruction execution cycle, explaining what is done in each phase. Draw the flow chart presenting initial configuration for the instruction cycle showing how the control determines the instruction type after the decoding.

b) A computer uses a memory unit with 512K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts:
   - an indirect bit
   - an operation code
   - a register code part to specify one of 32 register and
   - an address part
   - i) How many bits are there in op code, the register code part and address part?
   - ii) Draw instruction word format and indicate the number of bits in each part.
   - iii) How many bits are there in data and address input of the memory?

(9+6)

8.

a) Why do computers use addressing mode techniques? What is immediate addressing mode? Give the example of it.
   Explain the following with examples:
   - i) Indexed Addressing Mode
   - ii) Relative Addressing Mode
   - iii) Base Register Addressing mode

b. Write an assembly language (8086) program to find the largest number from the list of ten numbers defined as word at NUM. Put the result at LAR, which is defined as word.

(9+6)

9. Write short notes on the following:
   - i) Hardware algorithm to multiply two numbers, given in Sign-magnitude form
   - ii) Cache memory

(8+7)