A4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2. **PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein.   (1x10)

1.1 Which one among the following 2 Input logic gates can be used to implement any other 2 Input Logic gates?
A) AND
B) EX-OR
C) OR
D) NOR

1.2 What is the FAN-OUT of any standard TTL Logic Gate?
A) 2
B) 1
C) 10
D) 5

1.3 The 16's complement or F's complement of the HEX Number -2AB will be
A) 0FAC
B) FD55
C) FD54
D) EE55

1.4 Which among the following F/Fs is best suited to implement any synchronous counter?
A) J-K F/F.
B) T F/F
C) D F/F
D) S-R F/F

1.5 How many Half Adder Blocks are needed to implement a 1 bit Full Adder?
A) 2
B) 1
C) 3
D) 4

1.6   In order to access an Array element in any assembly language instruction, which among the following addressing modes happens to be most suitable?
A)   Memory Direct.
B)   Memory Indirect.
C)   Register Indirect.
D)   Based Indexed.

1.7   Within any CPU, the special purpose register provided to access the Stack Memory is termed as
A)   Instruction Pointer.
B)   Memory Data Register.
C)   Stack Pointer.
D)   Memory Address Register.

1.8   Multiplication Algorithm as supported by any Hardware Unit is essentially composed of which essential steps?
A)   Left Shift and Subtraction.
B)   Right Shift and Subtraction.
C)   Left Shift and Addition.
D)   Right Shift and Addition.

1.9   For any Peripheral Device like Disk, whose Data Transfer Rate to Memory can be faster than the rate at which the CPU can handle, which among the following Data Transfer Techniques happens to be most suitable?
A)   Interrupt Driven.
B)   Polling.
C)   DMA.
D)   None of the above.

1.10   Which among the following technologies is employed to build the Main Memory of modern day Laptops and PCs?
A)   Static RAM.
B)   Magnetic RAM.
C)   Dynamic RAM.
D)   Flash Memory.

2. **Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" answer sheet supplied with the question paper, following instructions therein.** **(1x10)**

2.1 EX –OR gate is the building block of any Adder.

2.2 Preset Input in a D F/F can be used to set its output to 0 asynchronously.

2.3 In Binary 2's complement scheme there exists separate representations for +0 and -0.

2.4 Tri-State control is necessary only at the output ports of each & every storage item that is connected to a shared bus.

2.5 Instruction cycle refers to the time taken by the CPU in fetching any machine coded instruction completely from the concerned memory.

2.6 Memory Address Register & Memory Data Register together represent the gateway for the CPU to the external world of memory & peripherals.

2.7 Overflow Flag in any CPU is relevant for unsigned operands only.

2.8 Interrupt driven data transfer is an Asynchronous mode of Data Transfer.

2.9 Cache memory is actually a static RAM.

2.10 Address operand in any 8086 instruction happens to be 20 bit wide.

3. **Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein.** **(1x10)**

	X		Y
3.1	3 Inputs and 8 Outputs Combinational Circuit	**A.**	-8
3.2	Inverter is another way to call	**B.**	A NOT Gate.
3.3	Both Inputs fed with 1 will represent an Unstable state in a	**C.**	256 number of different machine op codes.
3.4	1000 in 4 bit two's complement will have a Decimal Equivalent	**D.**	An OR Gate
3.5	ALU happens to be	**E.**	A mixture of combinational and sequential circuit blocks.
3.6	8 bit wide Machine Op Code will lead to	**F.**	Only Arithmetic Right shifting of the Partial Result
3.7	Data Transfer Instruction can possess maximum	**G.**	Is speed compatible with CPU
3.8	In Booth's multiplication algorithm a stream of 0s or 1s will cause	**H.**	Subtraction of Multiplicand from the partial result.
3.9	In order to transfer Data from a slow device to CPU	**I.**	2 Operand Addresses.
3.10	Cache Memory	**J.**	Handshaking mechanism must be there.
		K.	S-R F/F.
		L.	A purely combinational circuit.
		M.	3 to 8 Decoder

4. **Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein.** (1x10)

A.	Storage	B.	Content	C.	Instruction
D.	Segmented	E.	Edge	F.	Data
G.	Right	H.	1 Giga	I.	1 Mega
J.	Indirectly	K.	Asynchronous	L.	Logic '1'
M.	EX-OR				

4.1   In TTL +ve logic 5 Volt is treated as _____.

4.2   For single binary bit comparison _____ gate can be used.

4.3   _____ Triggering is preferred for building D F/Fs.

4.4   No ALU possesses any form of _____ element.

4.5   Cache Memory is usually _____ addressable.

4.6   In a 4 Gbyte memory having 32 bit Word size can actually store _____ distinct 32 bit words.

4.7   In 8086 _____ addressing is used to access any memory element.

4.8   All types of peripheral data transfer employs _____ mode of operation.

4.9   For dividing a binary integer by decimal 8, shift it _____ by 3 bits.

4.10   In the Assembly instruction JUMP TARGET the operand TARGET refers to an _____ address.

PART TWO
(Attempt any **FOUR** questions)

5.

a) Specify the Truth Table of a 1 bit Binary Full Adder that can be used to ADD single bit binary numbers x and y as well as a carry input c_{in} to produce the result bit z along with carry output c_{out}.

b) Use the Truth Table of (a) to implement the Binary Full Adder that ADDs single bit binary numbers x and y as well as a carry input c_{in} to produce the result bit z along with carry output c_{out} using 2 Level AND-OR Logic Circuit. Specify ALL design steps.

(8+7)

6. Using J-K F/Fs, specify the Logic structure of the ith stage of an n- bit Universal Register cum Counter in which the user based on a set of Control Inputs will be able to configure it in one from among the following mode.

i) Load from External Input.
ii) Shift LEFT the stored bit pattern by 1 bit.
iii) Shift RIGHT the stored bit pattern by 1 bit.
iv) Count UP.
v) Count Down.

You are to specify all the key DESIGN Steps along with relevant premises and assumptions as well as BLOCK Level Diagram.

(15)

7.

a) Specify the brief steps of the Booth's algorithm when employed to multiply two 4 bit signed (2's complement) binary numbers. A ($a_3a_2a_1a_0$) and B ($b_3b_2b_1b_0$) where a_3 and b_3 happen to be the respective signs.

b) Illustrate the actions of that algorithm in a stepwise fashion when it is used to multiply -7 (decimal) with $+5$ (decimal).

(7+8)

8.

a) Just by consulting the instruction set of any CPU, is it possible to ascertain whether the CPU possesses a separate I/O space? Justify your answer with examples.

b) During execution of an instruction by the CPU the following requests come simultaneously from several peripheral devices.

i) DMA request.
ii) Interrupt request.
iii) RDY signal from a slow Input Device.

Clearly specify the actions that the CPU will take. In what order the aforesaid requests will be served and why?

(3+12)

9. In a computer system, a 2 K byte of RAM module is to be implemented using 128 x 4 bit RAM chips. The CPU possesses a 20 bit address bus and a data bus of 8 bit width.

a) How many such chips will be needed and there will be how many pins at the minimum on each chip? Clearly depict ALL calculation. What will be the relevant pin signals? Justify & label the presence of each of them.

b) Does there exist any mechanism by which the given 2K RAM space can be placed anywhere in the 20 bit Address space? Discuss in brief about the same.

(12+3)