

ASIC DESIGN –AN1625

1. What is CMOS technology & write its advantages?

1. combination of both NMOS and PMOS.
2. uses the polysilicon gate.

Advantages:

1. Power consumption is less.

2. write the difference between custom IC and std IC?

Std IC:

Directly got from the market RAM, ROM, DRAM >

Custom IC:

Meant for specific application lot of std. IC combined to form a custom IC.

3. Write the example of IC's?

- * SRAM
- * DRAM
- * ROM

4. write some example of ASIC's?

- * The chip inside the toy.
- * Chip for a satellite.

5. What is meant by full custom ASIC's?

1. All the logic cells are customized.
2. All the mask layers that are customized.
3. Manufacturing is too difficult.

6. Write the different type of ASIC's?

1. Full custom ASIC.
2. Semicustom ASIC.
3. Programmable ASIC.

7. What is meant by CBIC?

CBIC means Cell Based ASIC.

- All the Mos layers are customized.
 - Custom blocks can be embedded.
 - Manufacturing lead time about 8 weeks.
- Ex: Flipflop, multiplexer, OR gate, AND gate.

8. Write the important features of CBIC?

* Designers can save money and time is reduced by using predesigned, pretested and precharacteristic.

* Logic cells can be optimized individually.

* Transistors are chosen to maximize or minimize the speed.

9. Define the term feedthrough?

The term feedthrough can refer either to the piece of metal that is used to pass a signal through a cell or to a space in a cell waiting to be used as a feedthrough.

10. What is meant by gate array based IC and write its type?

- * The transistors are predefined on the silicon wafer.
- * Predefined transistors on the gate array is known as base array.
- * The smallest element that can be replicated to form the base array is called base cells.
- * Number of layers .

*Bottom layers consists of transistors.

Type

- Channeled gate array
- Channeless gate array
- Structured gate array

11. What are the important parts in the datapath library?

A datapath library typically contains cells such as adders, subtractors, multipliers & simple Arithmetic And Logical Units.

12. Define structure gate array?

* Only the interconnections are customized.

* custom blocks can be embedded.

* Manufacturing lead time is between two days and two weeks.

13. What is difference between channeled and channeless gate array?

Channeless gate array:

No predefined areas between row and std cells.

Logic density of the channeless gate array is high

Contact mask is customized in the channeless gate array.

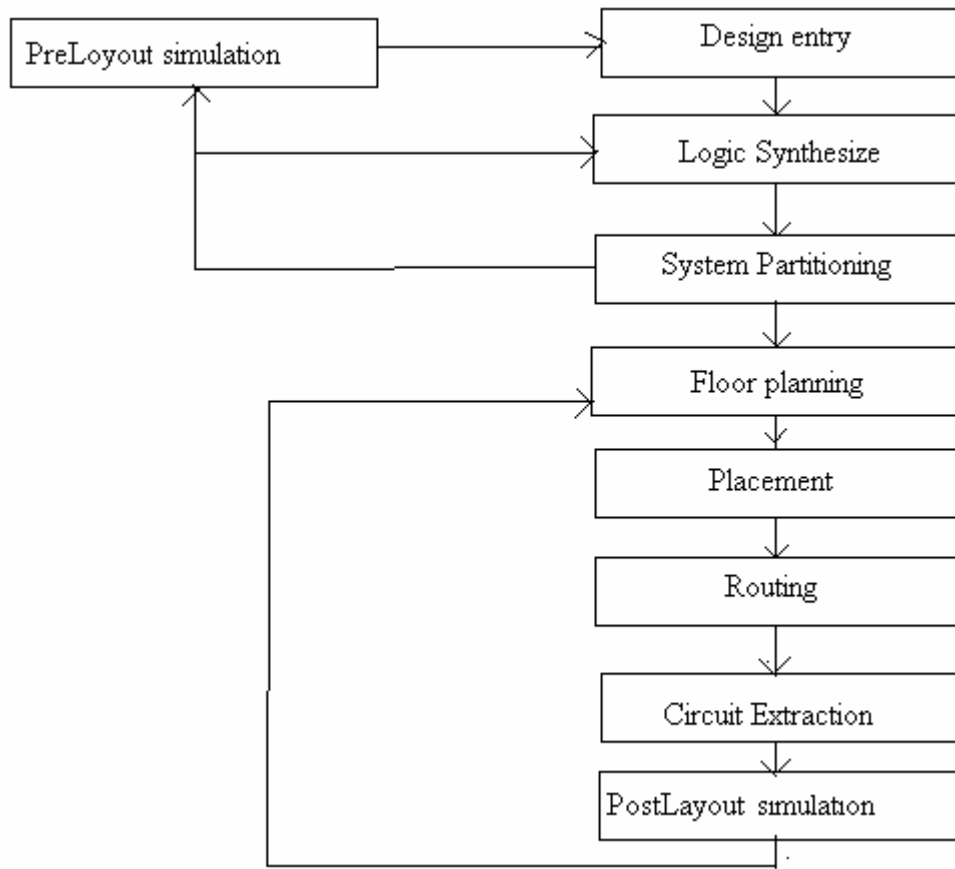
Channeled gate array:

predefined areas between row and std cells.

Logic density of the channeless gate array is low.

Contact mask is not customized in the channeless gate array

14. Write the design flow of an ASIC?



15. Define the transit time?

Time is taken by electron travel from source to drain. This is called as the transit time.

16. What is meant intrinsic transconductance & transistor gain factor?

Intrinsic Transconductance

$$k_n' = \mu_n C_{ox}$$

Where k_n' = Intrinsic transconductance

Gain factor

$$\beta_n = k_n' W/L$$

5. What is the difference between EEPROM and UVPRM technology?

EEPROM

*An electric field is used

rays are used

To remove electrons
From the floating gate
Of a programmed transistor.

UVPRM

The ultra violet

*This is faster than using a UV
to be removed from the system.

The chip have

Lamp and the chip doesnot
Have to be removed from
The system.

6. what is meant by PREP benchmarks

The programmable Electronics Performance Company (PREP) is a non profitable organization that organized a series of benchmarks for programmable ASICs.

7. Write some PREP benchmarks

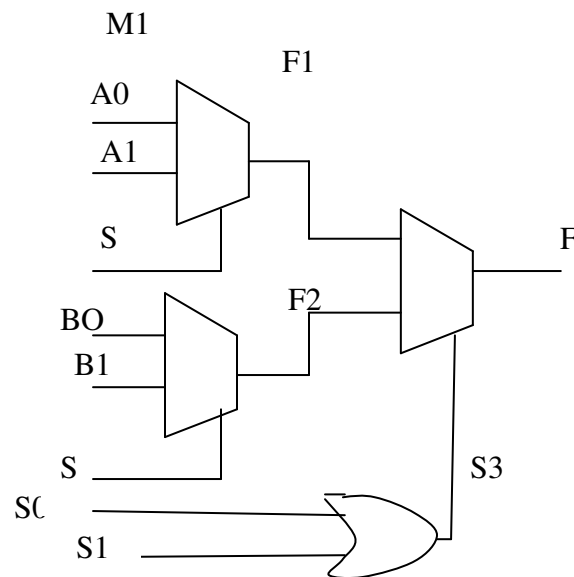
*An 8-bit datapath consisting of 4:1 MUX register and shift register.

*An 8 bit timer-counter consisting of two registers, a 4:1 MUX, a counter and a comparator

*A small state machine (8 states,8inputs,8outputs)

*A large state machine (16 states,8inputs,8outputs)

8. Draw the ACT1 logic module



9. write the Shanon's expansion theorem

Using the Shannon's expansion theorem, we can expand a Boolean logic function F in terms of a Boolean variable A ,

$$F = A \cdot F(A=1) + A' \cdot F(A=0)$$

Where $f(A=1)$ represents the function F evaluated with A set equal to '1'.

10. What is the difference between act2 and act3 logic modules

Act2 and Act3 architectures use a different types of logic modules. The logic module of act2 includes the equivalent of a D flip flop.

11. Define DC output

Driving a resistive load at a DC or low frequency (less than 1MHz)

Example loads are:

- *Light Emitting Diodes(LEDs)
- *Relays
- *Small motors

12. What is meant by AC output?

Driving a capacitive load with a high-speed (greater than 1MHz) logic signal off-chip.

Example loads are:

- *other logic chips
- *a data or address bus, ribbon cable.

13. Write the important input output requirements

- *DC output
- *AC output
- *DC input
- *AC input
- *clock input
- *power input

14. Define Dc input

Driving a resistive load

Example sources are:

- *switch
- *sensor or another logic chip

15. Define power input

We need to supply power to the I/O cells and the logic in the use, without introducing voltage drops or noise. We may also need a

Separate power supply to program the chip.

16. What is meant by derating factor?

To convert nominal or typical timing figures to worst case timing figures we use measured or empirically derived constants called derating factors.

17. Define critical path

Minimum delay path between the registers is called critical path.

18. Define worst case timing

Designers thus need to know the maximum delays they may encounter, which we call the worst case timing.

19. What is meant by speed grading

*Most of the FPGA header short chip according to speed is called speed binning or speed grading.

20. Define a. Logic expander

b. Programmable inversion

Logic expander

*The logic expander to generate extra logic terms, it possible to implement function that require more product term that are available in the simple PAL macrocell.

Programmable inversion

*Programmable inversion can be reduce the required number of product terms by using a DeMorgans equivalent representation

Instead of a conventional sum of products.

1. What are the materials used for building the interconnect?

Aluminum-based metallization, which has the sheet resistance of 50 m Ω /square and a line capacitance of 0.2pf/cm.

2. Write some points about ActelAct interconnect architecture?

It is similar to Channeled Gate Array. The channel routing uses dedicated rectangular areas of fixed size within the chip called wiring channels. The horizontal

channels run across the chip in the horizontal direction. In the vertical direction there are similar vertical channels that run over the top of the basic logic cell.

3. Define segmented channel routing?

To allow programming of the interconnect, Actel divides the fixed interconnect wires within each channel into various lengths or wire segments. This is called segmented channel routing.

4. What is meant by LVT and Output stub?

The single logic module output connects to a vertical track that extends across the two channels above the module and across the two channels below the module. This is the output stub. One vertical track per column is a long vertical track (LVT) that spans the entire height of the chip.

5. Write the Elmore's delay?

$$\text{Elmore's delay, } \tau_{Di} = \sum_{k=1}^n R_{ki} \cdot C_k$$

6. Define channel density?

It is the absolute minimum number of tracks needed in a channel to make a given set of connections.

7. What is meant by PIPs?

The Programmable Interconnect Points (PIPs) are Programmable pass transistors that connect the CLB inputs and outputs to the routing network.

8. What is meant by BIDA?

The Bidirectional Interconnect Buffers (BIDA) restore the logic level and logic strength on long interconnect paths.

9. Write some points about Xilinx EPLD architecture?

This family uses an interconnect bus known as Universal Interconnection Module (UIM) to distribute signals within the FPGA.

- CG is the fixed gate capacitance of the EPROM device.
- CD is the fixed drain parasitic capacitance of the EPROM device.
- Cw is the variable vertical bus capacitance.

10. Differentiate between Altera MAX 9000 and Altera FLEX interconnect architecture?

The MAX 9000 is a coarse-grained architecture. Complex PLDs with arrays that are themselves arrays of macrocells have a dual-grain architecture. The FLEX architecture is of finer grain than the MAX arrays because of the difference in programming technology. The FLEX horizontal interconnect is much denser than the vertical interconnect creating an aspect ratio of 10:1.

11. Define OEM?

For any ASIC, a designer needs design-entry software, a cell library and physical design software. Often designers buy that software from FPGA vendor. This is called an Original Equipment Manufacturer (OEM) arrangement.

12. Write some of the Low Level Language and High Level Language?

Low Level Languages-ABEL, CUPL, PALASM
High Level Languages-VHDL, VERILOG

13. Write File types used by the Actel Design Software?

ADL	Main Design Netlist
IPF	Partial or complete pin assignment
CRT	Net criticality
VALIDATED	Audit information
COB	List of macros removed from design
VLD	Information, Warning
PIN	Complete pin assignment
DFR	Information about routability
LOC	Placement and routing
PLI	Feedback from placement step
SEG	Assignment of horizontal routing segments
STF	Back annotation Timing
RTI	Feedback
FUS	Fuse coordinates
DEL	Delays for input pins
AVI	Fuse programming times

15. What are the different methods of Logic Minimization?

Logic Minimization can be done by either using a set of rules or using algorithms. Two level and multilevel logic minimization is implemented using CBIC, MGA, PLD.

16. Compare between Xilinx LCA, Actel Act and AlteraMAX architecture?

1. The Xilinx LCA architecture does not permit an accurate timing analysis until after place and route. This is because of the coarse-grained nondeterministic architecture.

2. The Actel Act architecture is nondeterministic, but the fine grained structure allows fairly accurate preroute timing prediction.

3. The Altera MAX complex PLD requires logic to be fitted to the product steering and PAL. The Altera MAX 7000 has a deterministic architecture , which allows accurate preroute timing.

17. Define Netlist?

The circuit schematic is a picture, an easy format to understand and use, but computers need to work with an ASCII or binary version of the schematic that we call a netlist.

18. Define Schematic Entry?

The schematic shows how all the components are connected together , the connectivity of an ASIC. This type of design entry process is called Schematic entry.

19. Define Hierarchical design?

Hierarchical design reduces the size and complexity of a schematic. To clarify the relationship between different levels of Hierarchy, we say that a subschematic is child of the parent schematic.

20. Write the components present in the schematic library?

Most ASIC companies provide a schematic library of primitive gates to be used for schematic entry. Library cells that represent basic logic gates are known as primitive cells. There are two types of macros for MGAs and Programmable ASIC. One is hard macro that includes placement information and the other is Soft macro contains only connection information.

1) Write one example for combinational logic in verilog

Two input AND gate

```
Module And-Always(X, Y, Z);
Input X, Y;
Output Z;
Reg Z;
Always @(X or Y)
Z<= X or Y;
//Combinational method 1
end module
```

2) Write the program for multiplexer in verilog

```
Module mux 8to1 (i,s,out) ;
Input[0:7]I;
Input[0:3]s;
Output out;
Reg out;
Always @(s or i)
Begin
Case(s)
3'b000:out=i[0];
3'b001:out=i[1];
3'b010:out=i[2];
3'b011:out=i[3];
3'b100:out=i[4];
3'b101:out=i[5];
3'b110:out=i[6];
3'b111:out=i[7];
Default : $ display (“invalid control signal”);
End case
End
End
```

3) Write the program for adder inVHDL

```
Library IEEE;
Use IEEE.NUMERIC-STD.all;
Use IEEE.STD-LOGIC-1164.all;
Entity adder-1 is
Port(A,B:in UNSIGNED(3 down to 0);
C:out UNSIGNED(4 down to 0);
End adder-1;
Architecture synthesis -1 for adder-1 is
Begin c<=('0'&A)+('0'&B);
End synthesis -1;
```

4) What are the types of simulation?

- ❖ Behavioral simulation
- ❖ Functional simulation
- ❖ Logic or gate level simulation
- ❖ Switch level simulation
- ❖ Transistor level simulation

5) Define behavioral simulation

One method models large pieces of a system as black box with input & output. This type of simulation called behavioral simulation.

6) What is functional simulation?

Functional simulation ignores timing and includes unit delay simulation, which sets delay to a fixed value.

7) What is static timing analysis

One class of simulators employed timing analysis that analysis logic in a static manner, computing the delay timing for each path. This is called static timing analysis because it does not required the creation of set of test vectors.

8) Define gate level simulation

It can be also used to check the timing performance of an ASIC. In a gate level simulation a logic gate or logic cell is treated as a black box modeled by a function whose variable are single inputs. The function also mode the delay through the logig cell setting all the delay value to unit value is the equalent of functional simulation.

9) Define transistor-level simulation

The most accurate but also the most complex & time consuming form of simulation is transistor level simulation.

10) What is mean by boundary scan test?

BST is the method for testing boards using a four wire interface. A good analogy would be the RS-232 interface for PCS. The PST standed interface was designed to test board, but also it used in ASIC.

11) What are the signals used in BST

- ❖ TDI-test data input
- ❖ TDO-test data output
- ❖ TCK-test clock
- ❖ TMS-test mode select

12) Draw the diagram of BST cells

13) Write the different type of faults

- ❖ Stuck at-1 fault

❖ Stuck at-0 fault



14) What is meant by parallel fault simulation?

Parallel fault simulation takes advantages of multiple bits of the words in the computer memory. In the simplest case we need only one bit to represent either a '1' or '0' for each node in the circuit. We would expect parallel fault simulation to be about 32 times faster than serial simulation

15) What is meant by nondeterministic fault simulation?

Some type of fault cannot be deterministic called as nondeterministic fault simulation.

16) What is the use of ATPG algorithm

The automatic test pattern generation used to generate some of the test vector.

17) Define PODEM algorithm and its advantages

The path-oriented decision making algorithm solves problem of reconvergent fanout and allows multipath sensitization. The method is similar to the basic algorithm.

18) What are the nine logic values used in VHDL

Logic state	Logic value
0	strong low
1	strong high
L	weak low
H	weak high
Logic state	Logic value
X	strong unknown
W	weak unknown
Z	high impedance
-	don't care
U	uninitialization

19) What is the use of test program?

The test program is used to measure the ASIC test program.

1) What are the goals and objectives of system partitioning?

The goal of partitioning is to divide the part of the system so that each partition is a single ASIC. The objectives are:

- i) A maximum size for each ASIC.
- ii) A maximum number for each ASIC.
- iii) A maximum number of connections for each ASIC.
- iv) A maximum number of total connections between all ASIC.

2) What is meant net cutset and edge cutset?

When we divide the network into two by drawing a line across connections we make net cuts. The resulting set of net cuts is the net cutset.

When we divide the network graph into the same partitions we make edge cuts and we create the edge cutset.

3) What are the different algorithms used for system partitioning?

The different algorithms used for system partitioning are:

- i) Constructive partitioning.
- ii) Iterative partitioning.

4) Write some of the iterative partitioning algorithms?

The Kernighan – Lin Algorithm.

The Ratio-cut Algorithm

The look-ahead Algorithm

Simulated annealing

5) What is meant by group migration?

Group migration comes under iterative partitioning improvements algorithms and consists of swapping groups of logic cell between partitions. The group migration algorithms are better than simple interchange methods.

6) Define global minimum?

Global minimum is the best solution for a given problem. It is the minimum value from a set of minimum values of a corresponding possible solutions.

7) What is meant by timing constraints and power constraints?

8) Write the goals and objectives of floor planning?

The goals of floor planning are to :

arrange the blocks on a chip

decide the location of the I/O pads

decide the location and number of the power pads

the objectives are to minimize the chip area and delay.

9) Define Channel definition?

In the floorplanning step we assign the areas between blocks that are to be used for interconnect. This process is known as channel definition or channel allocation.

- 10) What is an uncommitted feedthrough?
An unused vertical track (or just track) in a logic cell is called uncommitted feedthrough.
- 11) Write the goals and objectives of placement?
Goal is to arrange all the logic cells within the flexible block on a chip.
Objectives:
 Guarantee the router can complete the routing step.
 Minimize all the critical net delays
 make the chip as dense as possible
 minimize power dissipation
 minimize cross talk between signals
- 12) What is meant by rectilinear routing?
Rectilinear routing is the one in which all the interconnects are placed on a rectangular grid. This type of routing is also called Manhattan routing.
- 13) Define MRST?
The minimum rectilinear Steiner Tree (MRST) is the shortest interconnect using a rectangular grid.
Two approximation to MRST are complete graph measure and half perimeter measure
- 14) Write some of the placement algorithm?
Some of the placement algorithm are:
 min-cut algorithm
 eigen value method
 pairwise-interchange algorithm
- 15) Define hooke's law?
Hooke's law states that the force of a spring is proportional to its extension
- 16) Abbreviations of SDF, PDEF, LEF, RSPF, PEF and DSPF.
- 17) What is meant by global routing and detailed routing?
- 18) Goals and objectives of Global routing?
- 19) Define Back annotation.
- 20) What are the different design checks used in ASIC?

