

**NOORUL ISLAM COLLEGE OF ENGINEERING, KUMARACOIL  
DEPARTMENT OF ECE**

# **EC 1401 – VLSI DESIGN**

**TWO MARK & BIG QUESTIONS WITH ANSWERS**

**COMPILED BY**

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## 2 MARK QUESTIONS & ANSWERS

1. What are four generations of Integration Circuits?
  - ❖ SSI (Small Scale Integration)
  - ❖ MSI (Medium Scale Integration)
  - ❖ LSI (Large Scale Integration)
  - ❖ VLSI (Very Large Scale Integration)
2. Give the advantages of IC?
  - ❖ Size is less
  - ❖ High Speed
  - ❖ Less Power Dissipation
3. Give the variety of Integrated Circuits?
  - ❖ More Specialized Circuits
  - ❖ Application Specific Integrated Circuits(ASICs)
  - ❖ Systems-On-Chips
4. Give the basic process for IC fabrication
  - ❖ Silicon wafer Preparation
  - ❖ Epitaxial Growth
  - ❖ Oxidation
  - ❖ Photolithography
  - ❖ Diffusion
  - ❖ Ion Implantation
  - ❖ Isolation technique
  - ❖ Metallization
  - ❖ Assembly processing & Packaging
5. What are the various Silicon wafer Preparation?
  - ❖ Crystal growth & doping
  - ❖ Ingot trimming & grinding
  - ❖ Ingot slicing
  - ❖ Wafer polishing & etching
  - ❖ Wafer cleaning.
6. Different types of oxidation?  
Dry & Wet Oxidation
7. What is the transistors CMOS technology provides?  
n-type transistors & p-type transistors.
8. What are the different layers in MOS transistors?  
Drain , Source & Gate
9. What is Enhancement mode transistor?  
The device that is normally cut-off with zero gate bias.
10. What is Depletion mode Device?  
The Device that conduct with zero gate bias.
11. When the channel is said to be pinched –off?  
If a large  $V_{ds}$  is applied this voltage with deplete the Inversion layer .This Voltage effectively pinches off the channel near the drain.
12. Give the different types of CMOS process?
  - ❖ p-well process
  - ❖ n-well process

- ❖ Silicon-On-Insulator Process
- ❖ Twin-tub Process

13. What are the steps involved in twin-tub process?

- Tub Formation
- Thin-oxide Construction
- Source & Drain Implantation
- Contact cut definition
- Metallization.

14. What are the advantages of Silicon-on-Insulator process?

- No Latch-up
- Due to absence of bulks transistor structures are denser than bulk silicon.

15. What is BiCMOS Technology?

It is the combination of Bipolar technology & CMOS technology.

16. What are the basic processing steps involved in BiCMOS process?

Additional masks defining P base region

- N Collector area
- Buried Sub collector (SCCD)
- Processing steps in CMOS process

17. What are the advantages of CMOS process?

Low power Dissipation  
High Packing density  
Bi directional capability

18. What are the advantages of CMOS process?

Low Input Impedance  
Low delay Sensitivity to load.

19. What is the fundamental goal in Device modeling?

To obtain the functional relationship among the terminal electrical variables of the device that is to be modeled.

20. Define Short Channel devices?

Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. With short channel devices the ratio between the lateral & vertical dimensions are reduced.

21. What is pull down device?

A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

22. What is pull up device?

A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

23. Why NMOS technology is preferred more than PMOS technology?

N-channel transistors has greater switching speed when compared to PMOS transistors.

24. What are the different operating regions for an MOS transistor?

- Cutoff region
- Non-Saturated Region
- Saturated Region

25. What are the different MOS layers?

- n-diffusion
- p-diffusion
- Polysilicon
- Metal

26. What is Stick Diagram?

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

27. What are the uses of Stick diagram?

- It can be drawn much easier and faster than a complex layout.
- These are especially important tools for layout built from large cells.

28. Give the various color coding used in stick diagram?

- **Green** – n-diffusion
- **Red**- polysilicon
- **Blue** –metal
- **Yellow**- implant
- **Black**-contact areas.

29. Compare between CMOS and bipolar technologies.

CMOS Technology	Bipolar technology
<ul style="list-style-type: none"> <li>• Low static power dissipation</li> <li>• High input impedance (low drive current)</li> <li>• Scalable threshold voltage</li> <li>• High noise margin</li> <li>• High packing density</li> <li>• High delay sensitivity to load (fan-out limitations)</li> <li>• Low output drive current</li> <li>• Low <math>g_m</math> (<math>g_m \propto V_{in}</math>)</li> <li>• Bidirectional capability</li> <li>• A near ideal switching device</li> </ul>	<ul style="list-style-type: none"> <li>• High power dissipation</li> <li>• Low input impedance (high drive current)</li> <li>• Low voltage swing logic</li> <li>• Low packing density</li> <li>• Low delay sensitivity to load</li> <li>• High output drive current</li> <li>• High <math>g_m</math> (<math>g_m \propto e^{V_{in}}</math>)</li> <li>• High <math>f_t</math> at low current</li> <li>• Essentially unidirectional</li> </ul>

30. Define Threshold voltage in CMOS?

The Threshold voltage,  $V_T$  for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current,  $I_{DS}$  effectively drops to zero.

31. What is Body effect?

The threshold voltage  $V_T$  is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

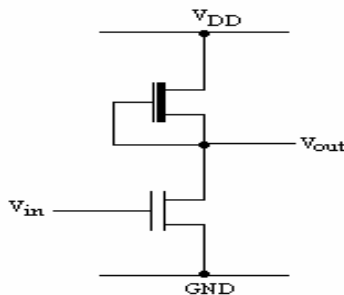
32. What is Channel-length modulation?

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied  $V_{DS}$ , increasing  $V_{DS}$  causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

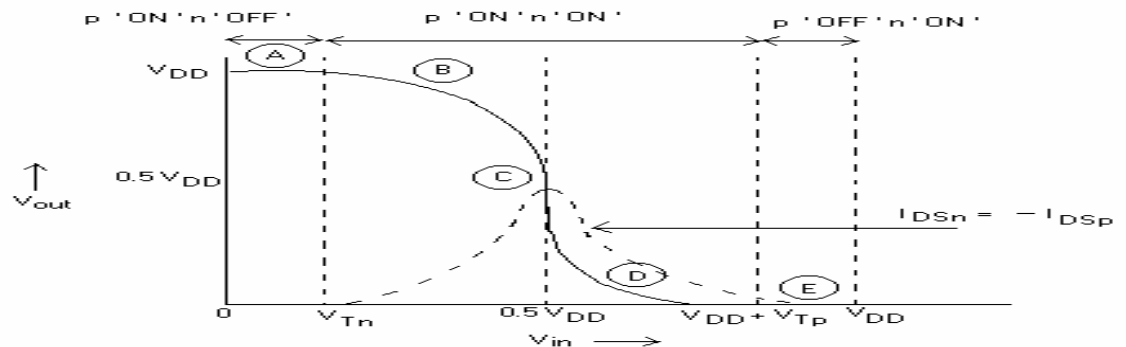
33. What is Latch – up?

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between  $V_{DD}$  and  $V_{SS}$  with disastrous results. Careful control during fabrication is necessary to avoid this problem.

34. Give the basic inverter circuit.



35. Give the CMOS inverter DC transfer characteristics and operating regions



36. Define Rise time

Rise time,  $\tau_r$  is the time taken for a waveform to rise from 10% to 90% of its steady-state value.

37. Define Fall time

Fall time,  $\tau_f$  is the time taken for a waveform to fall from 90% to 10% of its steady-state value.

38. Define Delay time

Delay time,  $\tau_d$  is the time difference between input transition (50%) and the 50% output level. This is the time taken for a logic transition to pass from input to output.

39. What are two components of Power dissipation.

There are two components that establish the amount of power dissipated in a CMOS circuit. These are:

- i) Static dissipation due to leakage current or other current drawn continuously from the power supply.
- ii) Dynamic dissipation due to
  - Switching transient current
  - Charging and discharging of load capacitances.

40. Give some of the important CAD tools.

Some of the important CAD tools are:

- i) Layout editors
- ii) Design Rule checkers (DRC)
- iii) Circuit extraction

41. What is Verilog?

Verilog is a general purpose hardware descriptor language. It is similar in syntax to the C programming language. It can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the switch level.

42. What are the various modeling used in Verilog?

- 1. Gate-level modeling
- 2. Data-flow modeling
- 3. Switch-level modeling
- 4. Behavioral modeling

43. What is the structural gate-level modeling?

Structural modeling describes a digital logic networks in terms of the components that make up the system. Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.

44. What is Switch-level modeling?

Verilog allows switch-level modeling that is based on the behavior of MOSFETs. Digital circuits at the MOS-transistor level are described using the MOSFET switches.

45. What are identifiers?

Identifiers are names of modules, variables and other objects that we can reference in the design. Identifiers consists of upper and lower case letters, digits 0 through 9, the underscore character(\_) and the dollar sign(\$). It must be a single group of characters.

Examples: A014, a ,b, in\_o, s\_out

46. What are the value sets in Verilog?

Verilog supports four levels for the values needed to describe hardware referred to as value sets.

<u>Value levels</u>	<u>Condition in hardware circuits</u>
0	Logic zero, false condition
1	Logic one, true condition
X	Unknown logic value
Z	High impedance, floating state

47. What are the types of gate arrays in ASIC?

- 1) Channeled gate arrays
- 2) Channel less gate arrays
- 3) Structured gate arrays

48. Give the classifications of timing control?

Methods of timing control:

1. Delay-based timing control
2. Event-based timing control
3. Level-sensitive timing control

Types of delay-based timing control:

1. Regular delay control
2. Intra-assignment delay control
3. Zero delay control

Types of event-based timing control:

1. Regular event control
2. Named event control
3. Event OR control
4. Level-sensitive timing control

49. Give the different arithmetic operators?

<u>Operator symbol</u>	<u>Operation performed</u>	<u>Number of operands</u>
*	Multiply	Two
/	Divide	Two
+	Add	Two
-	Subtract	Two
%	Modulus	Two
**	Power (exponent)	Two

50. Give the different bitwise operators.

<u>Operator symbol</u>	<u>Operation performed</u>	<u>Number of operands</u>
~	Bitwise negation	One
&	Bitwise and	Two
	Bitwise or	Two
^	Bitwise xor	Two
^~ or ~^	Bitwise xnor	Two
~&	Bitwise nand	Two
~	Bitwise nor	Two

51. What are gate primitives?

Verilog supports basic logic gates as predefined primitives. Primitive logic function keyword provide the basics for structural modeling at gate level. These primitives are instantiated like modules except that they are predefined in verilog and do not need a module definition. The important operations are and, nand, or, xor, xnor, and buf(non-inverting drive buffer).

52. Give the two blocks in behavioral modeling.
1. An initial block → executes once in the simulation and is used to set up initial conditions and step-by-step data flow
  2. An always block → executes in a loop and repeats during the simulation.
53. What are the types of conditional statements?
1. No else statement  
Syntax : if ( [expression] ) true – statement;
  2. One else statement  
Syntax : if ( [expression] ) true – statement;  
else false-statement;
  3. Nested if-else-if  
Syntax : if ( [expression1] ) true statement 1;  
else if ( [expression2] ) true-statement 2;  
else if ( [expression3] ) true-statement 3;  
else default-statement;  
The [expression] is evaluated. If it is true (1 or a non-zero value) true-statement is executed. If it is false (zero) or ambiguous (x), the false-statement is executed.
54. Name the types of ports in Verilog

**Types of port**

**Keyword**

Input port

Input

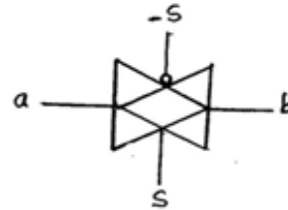
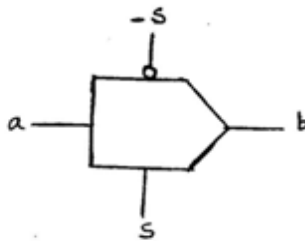
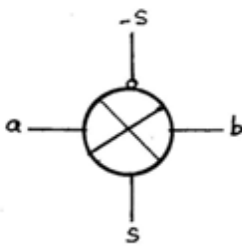
Output port

Output

Bidirectional port

inout

55. What are the types of procedural assignments?
1. Blocking assignment
  2. Non-blocking assignment
56. Give the different symbols for transmission gate.



57. Give the different types of ASIC.
1. Full custom ASICs
  2. Semi-custom ASICs
    - \* standard cell based ASICs
    - \* gate-array based ASICs
  3. Programmable ASICs
    - \* Programmable Logic Device (PLD)
    - \* Field Programmable Gate Array (FPGA).



58. What is the full custom ASIC design?

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

59. What is the standard cell-based ASIC design?

A cell-based ASIC (CBIC) USES PREDESIGNED LOGIC CELLS KNOWN AS STANDARD CELLS. The standard cell areas also called flexible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

60. Differentiate between channeled & channel less gate array.

**Channeled Gate Array**

**Channel less Gate Array**

- |  |  |
|--|--|
| 1. Only the interconnect is customized                                 | Only the top few mask layers are customized.                 |
| 2. The interconnect uses predefined spaces between rows of base cells. | No predefined areas are set aside for routing between cells. |
| 3. Routing is done using the spaces                                    | Routing is done using the area of transistors unused.        |
| 4. Logic density is less   | Logic density is higher.                                     |

61. Give the constituent of I/O cell in 22V10.

2V10 I/O cell consists of

1. a register
2. an output 4:1 mux
3. a tristate buffer
4. a 2:1 input mux

It has the following characteristics:

- \* 12 inputs
- \* 10 I/Os
- \* product time 9 10 12 14 16 14 12 10 8
- \* 24 pins

62. What is a FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

63. What are the different methods of programming of PALs?

The programming of PALs is done in three main ways:

- Fusible links
- UV – erasable EPROM
- EEPROM (E<sup>2</sup>PROM) – Electrically Erasable Programmable ROM

64. What is an antifuse?

An antifuse is normally high resistance ( $>100M\Omega$ ). On application of appropriate programming voltages, the antifuse is changed permanently to a low-resistance structure ( $200-500\Omega$ ).

65. What are the different levels of design abstraction at physical design.

- Architectural or functional level
- Register Transfer-level (RTL)
- Logic level
- Circuit level

66. What are macros?

The logic cells in a gate-array library are often called macros.

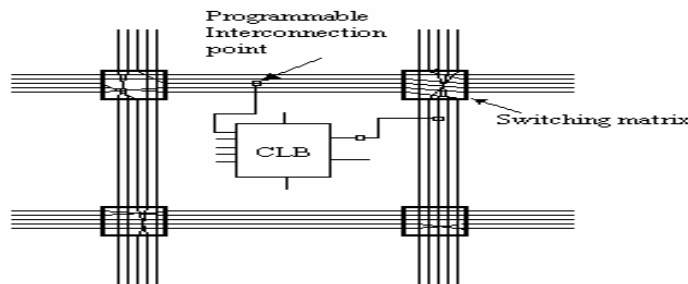
67. What are Programmable Interconnects ?

In a PAL, the device is programmed by changing the characteristics of the switching element. An alternative would be to program the routing.

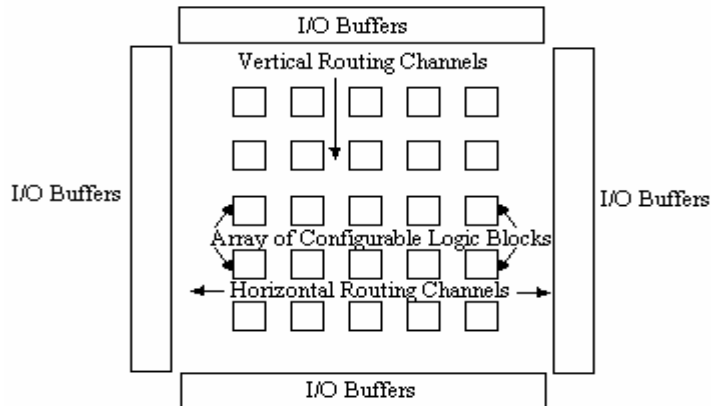
68. Give the steps in ASIC design flow.

- Design entry
- Logic synthesis System partitioning
- Prelayout simulation.
- Floorplanning
- Placement
- Routing
- Extraction
- Postlayout simulation

69. Give the XILINX Configurable Logic Block .



70. Give the XILINX FPGA architecture



71. Mention the levels at which testing of a chip can be done?
- At the wafer level
  - At the packaged-chip level
  - At the board level
  - At the system level
  - In the field
72. What are the categories of testing?
- Functionality tests
  - Manufacturing tests
73. Write notes on functionality tests?
- Functionality tests verify that the chip performs its intended function. These tests assert that all the gates in the chip, acting in concert, achieve a desired function. These tests are usually used early in the design cycle to verify the functionality of the circuit.
74. Write notes on manufacturing tests?
- Manufacturing tests verify that every gate and register in the chip functions correctly. These tests are used after the chip is manufactured to verify that the silicon is intact.
75. Mention the defects that occur in a chip?
- layer-to-layer shorts
  - discontinuous wires
  - thin-oxide shorts to substrate or well
76. Give some circuit maladies to overcome the defects?
- nodes shorted to power or ground
  - nodes shorted to each other
  - inputs floating/outputs disconnected
77. What are the tests for I/O integrity?
- I/O level test
  - Speed test
  - $I_{DD}$  test
78. What is meant by fault models?
- Fault model is a model for how faults occur and their impact on circuits.
79. Give some examples of fault models?
- Stuck-At Faults
  - Short-Circuit and Open-Circuit Faults
80. What is stuck – at fault?
- With this model, a faulty gate input is modeled as a “stuck at zero” or “stuck at one”. These faults most frequently occur due to thin-oxide shorts or metal-to-metal shorts.
81. What is meant by observability?
- The observability of a particular internal circuit node is the degree to which one can observe that node at the outputs of an integrated circuit.
82. What is meant by controllability?
- The controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state.

83. What is known as percentage-fault coverage?

The total number of nodes that, when set to 1 or 0, do result in the detection of the fault, divided by the total number of nodes in the circuit, is called the percentage-fault coverage.

84. What is fault grading?

Fault grading consists of two steps. First, the node to be faulted is selected. A simulation is run with no faults inserted, and the results of this simulation are saved. Each node or line to be faulted is set to 0 and then 1 and the test vector set is applied. If and when a discrepancy is detected between the faulted circuit response and the good circuit response, the fault is said to be detected and the simulation is stopped.

85. Mention the ideas to increase the speed of fault simulation?

- a. parallel simulation
- b. concurrent simulation

86. What is fault sampling?

An approach to fault analysis is known as fault sampling. This is used in circuits where it is impossible to fault every node in the circuit. Nodes are randomly selected and faulted. The resulting fault detection rate may be statistically inferred from the number of faults that are detected in the fault set and the size of the set. The randomly selected faults are unbiased. It will determine whether the fault coverage exceeds a desired level.

87. What are the approaches in design for testability?

- a. ad hoc testing
- b. scan-based approaches
- c. self-test and built-in testing

88. Mention the common techniques involved in ad hoc testing?

- d. partitioning large sequential circuits
- e. adding test points
- f. adding multiplexers
- g. providing for easy state reset

89. What are the scan-based test techniques?

- a) Level sensitive scan design
- b) Serial scan
- c) Partial serial scan
- d) Parallel scan

h. What are the two tenets in LSSD?

90. The circuit is level-sensitive.

- a. Each register may be converted to a serial shift register.

91. What are the self-test techniques?

- a. Signature analysis and BILBO
- b. Memory self-test
- c. Iterative logic array testing

92. What is known as BILBO?

Signature analysis can be merged with the scan technique to create a structure known as BILBO- for Built In Logic Block Observation.

93. What is known as IDDQ testing?

A popular method of testing for bridging faults is called IDDQ or current-supply monitoring. This relies on the fact that when a complementary CMOS logic gate is not switching, it draws no DC current. When a bridging fault occurs, for some combination of input conditions a measurable DC  $I_{DD}$  will flow.

94. What are the applications of chip level test techniques?

- a. Regular logic arrays
- b. Memories
- c. Random logic

95. What is boundary scan?

The increasing complexity of boards and the movement to technologies like multichip modules and surface-mount technologies resulted in system designers agreeing on a unified scan-based methodology for testing chips at the board. This is called boundary scan.

96. What is the test access port?

The Test Access Port (TAP) is a definition of the interface that needs to be included in an IC to make it capable of being included in a boundary-scan architecture. The port has four or five single bit connections, as follows:

- TCK(The Test Clock Input)
- TMS(The Test Mode Select)
- TDI(The Test Data Input)
- TDO(The Test Data Output)

It also has an optional signal

- TRST\*(The Test Reset Signal)

97. What are the contents of the test architecture?

The test architecture consists of:

- The TAP interface pins
- A set of test-data registers
- An instruction register
- A TAP controller

98. What is the TAP controller?

The TAP controller is a 16-state FSM that proceeds from state to state based on the TCK and TMS signals. It provides signals that control the test data registers, and the instruction register. These include serial-shift clocks and update clocks.

99. What is known as test data register?

The test-data registers are used to set the inputs of modules to be tested, and to collect the results of running tests.

100. What is known as boundary scan register?

The boundary scan register is a special case of a data register. It allows circuit-board interconnections to be tested, external components tested, and the state of chip digital I/Os to be sampled.

## BIG QUESTIONS & ANSWERS

1. Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.

Explanation (2)

Diagram (2)

CMOS inverter (2)

DC characteristics (5)

Transfer characteristics (5)

2. Explain with neat diagrams the various CMOS fabrication technology

P-well process (4)

N-well process (4)

Silicon-On-Insulator Process (4)

Twin- tub Process (4)

3. Explain the latch up prevention techniques.

Definition (2)

Explanation (2)

Diagram (2)

4. Explain the operation of PMOS Enhancement transistor

Explanation (2)

Diagram (2)

Operation (4)

5. Explain the threshold voltage equation

Definition (2)

Explanation (2)

Derivation (4)

6. Explain the silicon semiconductor fabrication process.

Silicon wafer Preparation (2)

Epitaxial Growth (2)

Oxidation (2)

Photolithography (2)

Diffusion(2)

Ion Implantation (2)

Isolation technique (2)

Metallization (1)

Assembly processing & Packaging (1)

7. Explain various CAD tool sets.

Layout editors (4)

Design Rule checkers (DRC) (4)

Circuit extraction (4)

8. Explain the operation of NMOS Enhancement transistor.

Explanation (2)

Diagram (2)

Operation (4)

9. Explain the Transmission gate and the tristate inverter briefly.

Explanation (2)

Diagram (2)

Operation (4)

10. Explain about the various non ideal conditions in MOS device model.

Explanation (2)

Diagram (2)

Operation (4)

11. Explain the design hierarchies.

Explanation (2)

Diagram (2)

Concept (2)

12. Explain the concept involved in Timing control in VERILOG.

Explanation (2)

Diagram (2)

Delay-based timing control (4)

Event-based timing control(4)

Level-sensitive timing control(4)

13. Explain with neat diagrams the Multiplexer and latches using transmission Gate.

Explanation (2)

Diagram (2)

Multiplexer (4)

latches(4)

14. Explain the concept of gate delay in VERILOG with example

Explanation (2)

Diagram (2)

Concept (2)

15. Explain the concept of MOSFET as switches and also bring the various logic gates using the switching concept .

Explanation (2)

Diagram (2)

Gate Concepts (4)

16. Explain the concept involved in structural gate level modeling and also give the description for Half adder and Full adder.

Explanation (2)

Diagram (2)

Gate Concepts (6)

Half adder (3)

Full adder (3)

17. What is ASIC? Explain the types of ASIC.

Definition (2)

Types (2)

Full custom ASICs (4)

Semi-custom ASICs(4)

Programmable ASICs(4)

18. Explain the VLSI design flow with a neat diagram

Explanation (2)

Flow Diagram (2)

Concepts (4)

19. Explain the concept of MOSFET as switches

Explanation (2)

Diagram (2)

Concepts (4)

20. Explain the ASIC design flow with a neat diagram

101. Design entry(2)

102. Logic synthesisSystem partitioning(2)

103. Prelayout simulation. (2)

104. Floorplanning(2)

105. Placement(2)

106. Routing(2)

107. Extraction (2)

2. Postlayout simulation(2)

21. a) Explain fault models.

Stuck-At Faults

Definition (2)

Diagram (2)

Short-circuit and Open-circuit faults

Definition (2)

Diagram (2)



- b) Explain ATPG.
  - Definition (2)
  - Truth tables (2)
  - Five valued logic (2)
  - Testability measures (2)
  
- 22. Briefly explain
  - a) Fault grading & fault simulation
    - Fault grading (2)
    - Fault simulation (2)
  
  - b) Delay fault testing
    - Diagram (2)
    - Description (2)
  
  - c) Statistical fault analysis
    - Definition (1)
    - Statistics (3)
  
  - d) Fault sampling (4)
  
- 23. Explain scan-based test techniques.
  - Level sensitive scan design (4)
  - Serial scan (4)
  - Partial serial scan (4)
  - Parallel scan (4)
  
- 24. Explain Ad-Hoc testing and chip level test techniques.
  - Ad-Hoc testing
    - Parallel-load feature (2)
    - Test signal block (2)
    - Use of the bus (2)
    - Use of multiplexer (2)
  - Chip level test techniques
    - Definition (2)
    - Regular logic arrays (2)
    - Memories (2)
    - Random logic (2)
  
- 25. Explain self-test techniques and IDDQ testing.
  - Signature analysis and BILBO (6)
  - Memory-self test (4)
  - Iterative logic array testing (3)
  - IDDQ testing (3)

26. Explain system-level test techniques.

Boundary scan – definition (2)

The Test Access Port (2)

The Test Architecture (2)

The TAP Controller (3)

The Instruction Register (2)

Test-Data Registers (2)

Boundary Scan Registers (3)