PART-A Questions

1. Convert $(10101100)_2$ into octal.
2. What is the important property of XS3 code?
3. What is the drawback of a serial adder compared to parallel adder?
4. Represent $(-10)_{10}$ in sign-2's complement form.
5. Mention any two applications of multiplexers.
6. Draw the logic diagram of a 2 x 4 decoder using NAND gates.
7. Define set-up time for a negative edge triggered FF.
8. Write the excitation table of a JK FF.
9. What is the basic difference between asynchronous sequential circuits and synchronous sequential circuits?
10. What is known as fundamental mode of operation of an asynchronous sequential circuit?
11. Convert $(196.062)_{10}$ to octal.
12. State the duality principle.
13. Draw the logic diagram of Half Subtractor.
14. What are the methods available in HDL?
15. Mention the uses of demultiplexer.
16. Draw the Logic Diagram of 4:1 multiplexer.
17. What is meant by Edge Triggered Flip Flop?
18. Give the excitation table of a T flip-flop.
19. What is primitive flow table?
20. What is one hot state assignment?
21. x + x'y = _____.
22. Convert $(BABA)_{16}$ to binary.
23. Represent 3124 in Excess-3-code.
24. When two n bit numbers are added and if it resulted in n+1 bits then _____ has occurred.
25. How many address lines and input output data are needed for the 8K*16 memory unit?
26. A decoder with an enable input can function as a _____.
27. The 4-bit shift register is initialized to 1011. What are the contents of the register after it is shifted six times to the right, with the serial input being 101111?
28. _____ is a level sensitive, one bit storage element.
29. What is a primitive flow table?

30. How to avoid critical races?
31. State De Morgan's Law.
32. Obtain the binary equivalent of hexadecimal number (AC.CB).
33. Name two HDL.
34. Draw the circuit for half adder.
35. What is ROM?
36. Define encoder.
37. What is latch?
38. Draw the truth table for T flip-flop.
39. What is asynchronous sequential logic?
40. Define hazards.

PART-B Questions

1. Write the absorption law and prove it.
2. Draw the logic diagram of a 4 bit binary to gray code converter using ex-OR gates.
3. Describe a 2 x 1 multiplexer using a HDL.
4. Write the HDL behavioral description of 4-bit universal shift register.
5. With an example explain static -1- hazard and its removal.
6. Define the laws of Absorption and Involution.
7. Design a combination circuit with three input variables that will produce a logic 1 outpu when more than one input variables are logic 1.
8. Compare PROM, PLA and PAL.
9. What is the difference between Moore and Mealy Circuit Models?
10. Explain the Hazards in combinational circuits?
11. Prove that $A'B'C' + A'BC' + AB'C' + ABC' = C'$
12. Design a 3 bit odd parity generator circuit.
13. Differentiate PLA and PAL.
14. Explain the operation of JK latch.
15. What is a flow table? Give an example.
16. State any three Boolean laws.
17. Draw the truth table and circuit for full adder.
18. Differentiate encoder and multiplexer.
19. Draw the circuit and truth table for D flip-flop.
20. What is race in asynchronous sequential logic circuits?

PART-C Questions

1. Simplify the following Boolean function using Karnaugh map and realize the simplified function using only NAND gates.

   F (a, b, c, d, e) = ∑m (1, 3, 4, 5, 11, 14, 15, 16, 17, 19, 20, 24, 26, 28, 30)

2. a. Convert the following Boolean function into product of maxterms form.

   F (a, b, c) = $(a+\bar{c})(\bar{a}+b+\bar{c})(\bar{a}+\bar{b})$

   b. Show that the dual of exclusive –OR is also its complement.

3. Design a single stage BCD adder and draw its block diagram.
4. Design a 4-bit carry-look-ahead adder and draw its block diagram.
5. Design an octal to binary priority encoder and draw its logic diagram using gates.
6. Draw the logic diagram of the realization of the following functions using a PAL device

   $F_1$ (a, b, c) = ∑m (1, 2, 4, 6, 7)

   $F_2$ (a, b, c) = ∑m (2, 4, 5, 6)

   $F_3$ (a, b, c) = ∑m (1, 4, 6)

7. a. Draw the block diagram of 4 bit universal shift register using FFs and multiplexers and explain its working.

   b. Compare a 4- bit binary counter and a 4-stage ring counter.

8. Design a synchronous modulo -5 up-down counter using JK FFs. Draw the timing diagram and write your inference.
9. a. Stage the three constraints that must be satisfied while designing an asynchronous sequential circuit to function properly.

   b. Explain the two types of race conditions using an example.

10. Obtain the primitive flow table and a minimum row flow table for a fundamental mode asynchronous sequential circuit with two inputs x and y, with a single output z, meeting the following requirement:

    The output z is 1, only when the values of inputs x and y are same and y was the variable that changed value causing both inputs to become the same.

11. Reduce the following expressions:

    a. $\bar{A}BC\bar{D}+BC\bar{D}+B\bar{C}\bar{D}+B\bar{C}D$

    b. $AB+\bar{A}\bar{C}+A\bar{B}C(AB+C)$

    c. What is the value of b if $\sqrt{44_b}=6$?

    d. Convert $(37.29)_{10}$ to octal and hexadecimal.

12. Reduce the following functions using K - Map techniques and implement using basic

gates

a. f(A, B, C, D, E) = ∑m(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + d(0, 12, 16, 17)

b. f(A, B, C, D) = π m(4, 5, 6, 7, 8, 12, 13) + d(1, 15)

13. a. Design and explain the operation of binary to BCD converter with K-Map and logic diagram.

b. Write a short note on Hardware Description Languages.

14. Explain the building of a 24 - bit magnitude comparator using 4 -bit comparator.

15. a. Explain the logic diagram of 3 to 8 line decoder.

b. How do you construct a 4 x 16 decoder with two 3 x 8 decoders.

16. Implement the following function using PAL.

W (A, B, C, D) =∑ m (2, 12, 13)

X (A, B, C, D) = ∑m (7, 8, 9, 10, 11, 12, 13, 14, 15)

Y (A, B, C, D) = ∑m (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)

Z (A, B, C, D) = ∑m (1, 2, 8, 12, 13)

17. Design a sequential circuit using JK flip-flop for the following state table [use stat diagram]

| Present state | Next state | | Outp ut | |
|---|---|---|---|---|
| AB | X=0 | X=1 | X=0 | X=1 |
| 00 | 00 | 11 | 1 | 0 |
| 01 | 01 | 11 | 1 | 1 |
| 10 | 01 | 00 | 1 | 0 |
| 11 | 11 | 10 | 0 | 0 |

18. a. Explain Serial in Serial out Shift Register.

b. Explain Serial in parallel out Shift Register.

19. Explain the classification of Race- Free State Algorithm.

20. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to outpu y. When B is 0, the output does not change, for any change in input.

21. Simplify the following Boolean functions using K map:

a. F=∑(0,5,7,13,15,16,21,23,25,29,31).

b. F=∑ (1,3,5,7,8,9,12,13).

22. a. Express the following function using sum of minterms and product of maxterm F(A,B,C,D ) = B'D+A'D+BD

b. Find the complement of $xy' + x'y$

23. What is carry propagation delay in Binary Adder? How can it be avoided using carry loc

ahead generator?

24. a. A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's.The output is 0 otherwise. Design a 3bit majority circuit.
    b. Write an HDL for a Half Adder circuit.
25. Design a four bit priority encoder with input $D_3$ having the highest priority and $D_0$ having lowest priority.
26. Implement the following function using PLA
    a. $F_1$=AB'+AC+A'BC'
    b. $F_2$=(AC+BC)'
27. Explain the Binary ripple counter using JK flip flop and T flip flop.
28. a. Explain the operation of master slave D-flip flop.
    b. Construct a JK flip flop using the following components: D flip flop, 2-to-1 multiplexers and an inverter.
29. Explain the analysis and design procedure of an Asynchronous sequential circuit.
30. Explain in detail about the Race free state assignments.
31. Simplify F = Σm (1, 3, 7, 11, 15) + d (0, 2, 5) using K-map.
32. What are universal gates? Design Ex-OR gate using NAND and NOR logic.
33. Design a full subtractor circuit.
34. Realize a BCD to Gray code conversion circuit starting from its truth table.
35. Explain with neat diagram a BCD to 7-segment display decoder.
36. Explain about PROM, PLA and PAL in detail.
37. Design and implement a Mod-10 synchronous counter using D flip-flop.
38. Explain about various types of shift registers in detail with neat diagrams.
39. Explain the design procedure of asynchronous sequential circuit with necessary steps.
40. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X.