Ex/PG/PE/T/1210A/201/2009

MASTER OF POWER ENGINEERING EXAMINATION, 2009

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MASTER OF SOFTWARE ENGINEERING EXAMINATION, 2009

(2nd Semester)

REAL-TIME EMBEDDED SYSTEMS

Time : Three hours Full Marks : 100

Answer any *five* questions.

1. a. For a 2-task system T_1, T_2 with periods P_1, P_2 ($P_1 < P_2$), priorities Γ_1, Γ_2 and execution times C_1 and C_2, show that if the task set is schedulable with $\Gamma_1 < \Gamma_2$, then the task set is schedulable with $\Gamma_1 > \Gamma_2$ and not vice-versa. 10

   b. Enumerate the assumptions for which 1a. is valid, 4

   c. Define critical instant, critical zone and tax laxity. 6

2. a. Using the data of 1a. above calculate the least upper bound of maximum processor utilization η for a schedulable task set assuming $\Gamma_1 > \Gamma_2$ 15

   b. Assuming RM scheduling calculate the limiting value of η for an infinite task set. (do not derive η) 5

3. a. Tabulate the differences between Round-Robin, Interrupt-Driven and RM scheduling in a RTOS. 6

   b. What are the requirements of a RTOS? 2

   c. A real-time embedded system is developed around an intel 8088 based system with a single 8259. It comprises three tasks T1, T2 and T3, with priorities in the same sequence which are connected to IRQs 4,5 and 6 respectively, with a default priority assignment for the IRQs. If the tasks are associated with execution times of 20, 25 and 30 msec. respectively, and the interrupt latency is 5 micro-sec., what is the response time of the system, if interrupt driven scheduling is assumed?

   If the period at which the triggers arrive is same and it is P, what should be the minimum value of P if no overflow occurs, assuming scheduling overhead is 10%? 12

4. a. Distinguish between
   (i) Counting and Flag semaphores
   (ii) Burst mode and FIFO mode semaphores 4

   c. 3 tasks T_1, T_2 and T_3, with priorities in the same sequence are synchronized using a flag semaphore. Initially, T_1 and T_2 are in the blocked state when T_3 runs for 50 ms after having set the semaphore, when it is pre-empted by T_2. T_2 runs for 30 ms. more before it is blocked again , while trying to set the same semaphore, and T3 runs for a further period of 10 ms. when it is pre-empted by T_1 which runs for 20 ms. and gets blocked again when it tries to set the semaphore set by T_1.T_3 then runs for 15ms. and resets the semaphore. If T_2 and T_1 take further 20 ms. each to complete the activities for the particular cycle, draw the execution profile and calculate the time spent by T_1 in blocked mode assuming a) a burst mode semaphore and b) a FIFO mode semaphore. Calculate η for the task-set. 16

[Turn over

5. a. With the help of a neat sketch explain how the interrupt type is established in a 8088 based system with a single 8259 and hence explain what is the minimum duration between two interrupts connected to the same IRQ if the clock frequency is F. 14

   b. Assuming the even address associated with the 8259 to be 20H, write the initialization sequence to program the 8259 with the following:
      (i) There is a single 8259
      (ii) The interrupts are Level Triggered with AEOI
      (iii) IRQ 5 has the highest priority 6

6. a. What is mark bit and stop bit for asynchronous serial communication? What is the relationship between their signs?. What is the significance of the mark bit? 6

   b. Assuming a base address write the instruction sequence to program a UART with the following:
      (i) 8 bit data, no parity, 2 stop bits
      (ii) Operation at 9600 baud
      (iii) Rx and Tx interrupts enabled
      (iv) Rx and Tx clock factor of 2 8
      (v)

   c. NS16550 is a better version of 8251 in which a FIFO(max. 16 element) is implemented and the interrupt is generated once the FIFO is filled upto a threshold. Calculate if the chip can be used to sink data at 19.2kbps in an interrupt driven mode, reading the FIFO in response to an interrupt takes 500 micro-sec. The data may be assumed to be 8 bit, no parity with 2 stop bits. 6

7. a. A CAN uses a data speed of 1 Mbps with a n bit data identifier and a m bit data length (inclusive of the identifier).Calculate the following:
      (i) arbitration time
      (ii) maximum delay in transmission of a higher priority message 10

   b. What is re-entrancy? What are the measures by which is ensured? How do you generate re-entrant code using an integrated development environment? 10

8. Two data streams $\mathbf{d_1}$ and $\mathbf{d_2}$ arising out of 2 independent sources undergo sequential data transformations D_1, D_2, D_3, D_4 and D_5 in response to a common periodic timer event e with a periodicity of P. The event e is generated by a task T_0 and the transformation D_5 is interfaced with D_4 using a synchronized buffer. Using DARTS, 20

   a. represent the system using DFD
   b. identify the tasks stating the criteria
   c. suggest a suitable priority assignment
   d. suggest a suitable synchronization mechanism for the synchronization specified in the problem