DHANALAKSHMI SRINIVASAN INSTITUTE OF RESEARCH AND TECHNOLOGY

Department of Computer science and engineering

CS6303 COMPUTER ARCHITECTURE

Question Bank

Year :II year

UNIT-1OVERVIEW AND INSTRUCTIONS

PART-B

1. **Discuss in detail about Eight great ideas of computer Architecture**.
    - Design for moore's law
    - Use abstraction to simplify designs
    - Make the common case Fast
    - Performance via parallelism
    - Performance via pipelining
    - Hierarchy of memories
    - Dependability via redundancy
    - Performance via predication.
2. **Explain the various components of computer System with neat diagram**.
    - Input devices
    - Output devices
    - Memory
    - CPU or processor
    - Network
3. **Discuss in detail the various measures of performance of a computer.**
    - Performance Evaluation

- Measuring performance
- CPU performance Equation
- SPEC CPU benchmark
  - Implementation of Amdahl's law

4. **Define Addressing mode and explain the basic addressing modes with an example for each.**
   - Immediate addressing
   - Register addressing,
   - Base or displacement addressing
   - PC-relative addressing
   - Pseudo direct addressing

5. **Explain operations and operands of computer Hardware in detail.**
   - operands of computer Hardware
   - compiling a C assignments using registers
   - memory operands
6. **Discuss the Logical operations and control operations of computer**.
   - Logical operations
     - Bitwise operation AND
     - Bitwise operation OR
   - Control operations
     - MIPS encoding for jump instruction
     - MIPS code
     - Compiling loop statements
     - Case/switch statements
     - Jump and link
     - Coprocessor instructions
     - Summarization of MIPS instruction format

UNIT-II ARITHMETIC OPERATIONS

1. **Explain the Multiplication algorithm in detail with diagram and examples**
    - Signed multiplication
    - Booth algorithm
    - Booth algorithm for Signed multiplication
    - Faster Multiplication
    - Multiply in MIPS
2. **Discuss in detail about division algorithm in detail with diagram and examples**.
    - Signed division
    - Faster division
    - Division in MIPS
        - Step 1: Test divisor<dividend.
        - Step 2: if divisor<dividend.
        - Step 1: shift the divisor right by 1 bit
3. **Explain in detail about floating point representation**
    - IEEE 754 standard
    - Scientific notation in binary
        - Single precision floating point IEEE 754 standard
        - Double precision floating point IEEE 754 standard
    - Normalization representation
        - Sizes
        - Sign bit
        - Exponent
        - Special values
        - Denormalized representation
    - Floating point under flow and over flow
    - Guard and rounding.

4. **Explain in detail about floating point arithmetic operation.**
    - Floating point addition and subtraction
    - Floating point addition
        - Procedure
        - Example
    - Floating point Multiplication
        - Procedure
        - Example
    - Floating point in MIPS
5. **Explain in detail about basic concepts of ALU design**
    - 1-bit ALU design
    - Full adder
    - 32-bit ALU design
    - MIPS ALU design
    - Arithmetic for multimedia
6. **Explain in detail about arithmetic operation**
    - Boolean addition
    - Boolean subtraction
    - Overflow
    - MIPS Overflow handling
    - Ripple carry adder
    - Fast adder circuit
    - Carry look ahead adder

UNIT III PROCESSOR AND CONTROL UNIT

1. **Explain the basic MIPS implementation of instruction set**
   - ✓ The memory –reference instruction load word(lw) and store word(sw)
   - ✓ The arithmetic –logical instruction add,sub,and,or,and slt
   - ✓ The instruction branch equal (beq) and jump (j)
     - Clocking methodology
2. **Explain in detail about building a data path**
   - Data path elements
   - Data path for branch instruction
   - Creating a single Data path
3. **Explain in detail about control implementation scheme**.
   - The ALU control
   - Designing the control unit
   - Operation of the Data path for an R type instruction
   - Finalizing the control
   - A multi cycle implementation
4. **What are control hazards? Explain the methods for dealing with the control hazards.**
   - Reducing the delay of branch
   - Pipeline branch
   - dynamic branch prediction
     - 1-bit prediction scheme
     - 2-bit prediction scheme
5. **Discuss the data hazards and forwarding in pipelining**

   1a) EX/MEM. RegisterRd =ID/EX. register RS

   1b) EX/MEM. RegisterRd =ID/EX. register RT

   2a) MEM/WB. RegisterRd =ID/EX. register RS

2b) MEM/WB. RegisterRd =ID/EX. register RT

- Dependence detection
  - Sub $1,$2,$3
  - add $1,$2,$3
  - or $1,$2,$3
- EX Hazards
- MEM Hazards

6. **How exceptions are handled in MIPS**
   - Instruction fetch and memory stages
     - Memory protection violation
   - Instruction decode stages
     - Undefined illegal opcode
   - Execution stage
     - Arithmetic exception
   - Write back stages

UNIT IV PARALLELISM

1. **Explain Instruction level parallelism**
   - Dynamic, hardware intensive approach
   - Static, complier intensive approach
   - Loop level parallelism
   - Data dependences and hazards
     - Data dependences
     - Control dependences
     - Structure dependences
   - ILP architecture

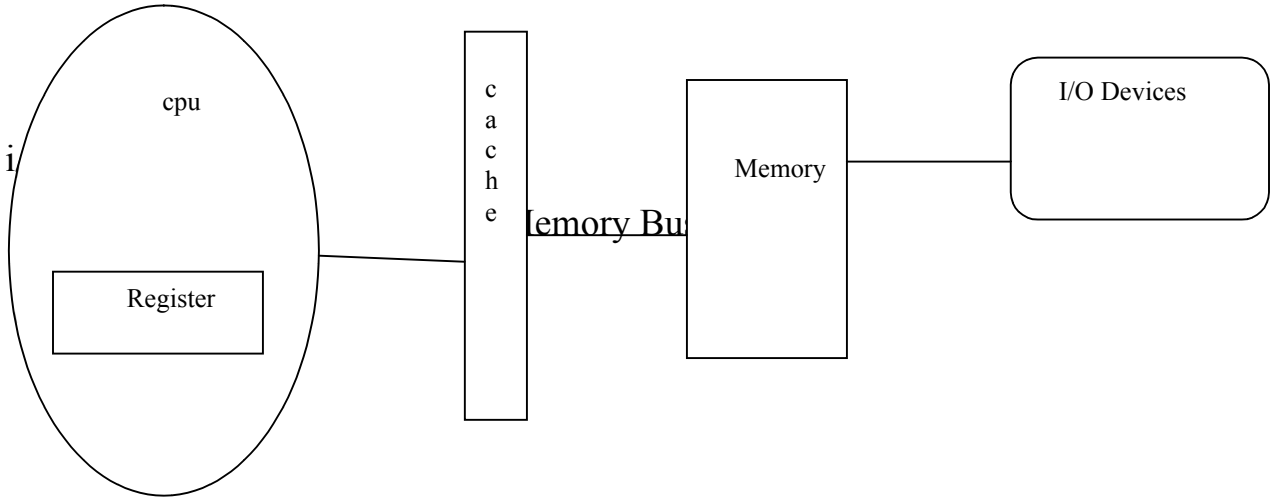
2. **Explain the difficulties faced by parallel processing programs**
    - First major challenges –goods speedup
    - Second major challenges –remote access in parallel processing
3. **Explain in detail Flynn's classification of parallel hardware**
    - Introduction
    - Flynn's taxonomy
    - Single instruction stream, single data stream (SISD)
    - Single instruction stream, multiple data stream (SIMD)
    - Multiple instruction streams, single data stream (MISD)
    - Multiple instruction stream, multiple data stream(MIMD)
4. **Explain in detail hardware Multithreading**
    - Fine grained multithreading
        - Advantages
        - Disadvantages
    - Coarse grained multithreading
        - Advantages
        - Disadvantages
    - SMT
        - A super scalar without multithreading
        - A super scalar Fine grained multithreading
        - A super scalar Coarse grained multithreading
        - A super scalar SMT multithreading
5. **Explain Multicotre processor**
    - Centralized shared memory architecture
    - Classification based on communication models
        - Distributed shared memory
        - Message passing multiprocessor

UNIT V MEMORY AND INPUT OUTPUT SYSTEMS

1. Explain in detail about memory hierarchy.

The principle of locality, states that program access a relatively small portion pof their address space at any instant of time.

- Temporal locality
- Spatial locality



2.Explain Memory Technologies

Main memory is the next level hierarchy

It satisfies the demand of caches and serves as I/o interface

Types

- SRAM
- CMOS
- DRAM
- SYCHRONOUS DRAM
- DOUBLE DATA RATE DRAM
- RAMBUS MEMORY
- ROM
- PROM

- EPROM
- EEPROM
- FLASH MEMORY
- FLASH CARD
- FLASH DRIVE

3.Explain about cache memory in detail

• Cache memory is a small amount of fast memory

∗ Placed between two levels of memory hierarchy

» To bridge the gap in access times

– Between processor and main memory (our focus)

– Between main memory and disk (disk cache)

How Cache Memory Works

• Prefetch data into cache before the processor needs it

∗ Need to predict processor future access requirements

» Not difficult owing to locality of reference

• Important terms

∗ Miss penalty

∗ Hit ratio

∗ Miss ratio = (1 – hit ratio)

∗ Hit time

4. Explain about DMA Conroller

DMA channel: DMA channel is issued to transfer data between main memory and peripheral device in order to perform the transfer of data. The DMA controller access rs address and data buses.

DMA with help of schematic diagram of controller on tile needs the dual circuits of and e to communicate with -CPU and I/O device. In addition, it nee s an address register; a word count register, and a set of, es The address register and address lines are used for communication with memory to word count

register specifies the no. of word that - must be transfer may be done directly between the device and memory .

5. Explain about 1/0 processor

Input/Output processor/information processor: It is designed to handle input/ output processes of a device or the computer. This processor is separate from the main processor (CPU). I/O processor is similar to CPU but it controls input output operations only. The computer having I/O processor relieves CPU from Input/output operations only. CPU is the master processor of the computer and it instructs the I/O processor to handle the input output tasks. I/O processor cannot work independently and is controlled by the CPU.

The I/O processor is composed of commercially available TTL logic circuits that generate the micro instructions necessary to implement the I/O instructions. The I/O processor is fully synchronous with the system clock and main processor. it receives starting control from the main processor (CPU) whenever an input output instruction is read from memory. The I/O processor makes use of system buses after taking the permission from the CPU. It can instruction the I/O processor 1/0 processor responds to CPU by placing a status word at prescribed location to be checked out by the CPU later on CPU informs the 1/0 processor to find out the 1/0 program and ask 1/0 processor to transfer the data. I/O

6. What are the advantages you got with virtual memory?

permit the user to construct program as though a large memory space were available, equal to totality auxiliary memory. Each address that is referenced by CPU goes through an address mapping from so called virtual address to physical address main memory.

There are following advantages we got with virtual memory:

1. Virtual memory helps in improving the processor utilization.

2. Memory allocation is also an important consideration in computer programming due to high cost of main memory.
3. The function of the memory management unit is therefore to translate virtual address to the physical address.
4. Virtual memory enables a program to execute on a computer with less main memory when it needs.
5. Virtual memory is generally implemented by demand paging concept In demand paging, pages are only loaded to main memory when they are required
6. Virtual memory that gives illusion to user that they have main memory equal to capacity of secondary stages media.

   The virtual memory is concept of implementation which is transferring the data from secondary stage media to main memory as and when necessary. The data replaced from main memory is written back to secondary storage according to predetermined replacement algorithm.