Code No: RR410506 **Set No. 1**

IV B.Tech I Semester Supplimentary Examinations, November 2008
FAULT TOLERANT SYSTEMS
(Common to Computer Science & Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) A computer system contains 10,000 components each with failure rate 0.5% per 1000 hours. What is the period of 0.99 reliability of this system. [6]
   (b) What is meant by active repair time and passive repair time referred in maintainability of a system. Derive the expression for the MTTR. [3+3+4]

2. (a) A circuit realizes the function.
   Z=$\overline{X_1}\ X_4$+$\overline{X_2}\ X_3$+$X_1\overline{X_4}$
   Using Boolean Difference method find the test vectors for SA0, SA1 faults on all input lines of the circuit.
   (b) What are the different properties of Boolean differences? Explain. [5+5+6]

3. (a) Design a redundant circuit for f = ab + $a'b'$
   (b) Explain the Dynamic redundancy Technique of a fault Tolerant system.[8+8]

4. (a) What is the mechanism adopted in COPRA a fault Tolerant system. Explain in detail.
   (b) What is meant by Time redundancy? Explain. [4+4+4+4]

5. Design a totally self-checking checker for maximal-length Berger codes also give the procedure to generate test vectors of 8 bit long. [8+8]

6. Explain the steps to derive G-functions which generates the $C_i(o \leq i \leq m)$ check bits in modified Berger code specially for detecting uni-directional output errors in PLAs. Take an example to explain the above steps. [16]

7. (a) Explain three level OR-AND-OR design technique.
   (b) Write a short note on adding control logic in to a combinational logic to have only 5 test pattern. [8+8]

8. (a) Draw the logic diagram of Hazard-free polarity hold latch, and explain with the help of flow table & excitation table. [2+2+2]
   (b) Draw the logic diagram of shift register latch and explain its principle. Using above latch. [3+7]

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Code No: RR410506 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) A computer system contains 10,000 components each with failure rate 0.5% per 1000 hours. What is the period of 0.99 reliability of this system. [6]
   (b) What is meant by active repair time and passive repair time referred in maintainability of a system. Derive the expression for the MTTR. [3+3+4]

2. (a) What is a tree live circuit. Give properties of tree like circuits.
   (b) For the given tree like circuit find the complete test set using path sensitizing method as show in figure 2b. [3+5+8]

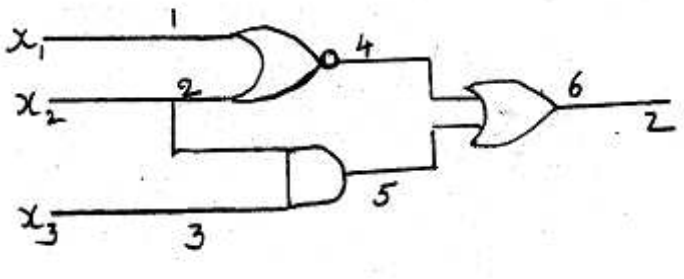

Figure 2b

3. (a) Construct a seven-bit error correcting code to represent the decimal digit by augmenting the Excess-3 code and by using add-1 parity check.
   (b) Design a redundant circuit for $f = a \oplus b$ [9+7]

4. (a) What is the mechanism adopted in COPRA a fault Tolerant system. Explain in detail.
   (b) What is meant by Time redundancy? Explain. [4+4+4+4]

5. (a) What is the need for self checking circuits
   (b) Design a totally self checking checker by using reddy's partition method for 2out of 5 code. [6+10]

6. Apply the procedure of designing a fail safe sequential machine using Berger code to the given state table. [16]

PS	NS, Z x=0	 x=1
A	E,0	B,0
B	C,0	D,0
C	A,0	D,0
D	E,0	D,1
E	A,0	D,1

7. Explain the technique for designing minimally testable network which produces a circuit which can be tested by three tests only.Modify the function $f = \overline{A}\ \overline{B}$C +A $\overline{B}\ \overline{C}$ into a circuit which has only three tests. [10+6]

8. (a) Explain how tristate drivers are used to improve testability.
   (b) Explain the scan path technique for Testable sequential circuit design. [8+8]

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Code No: RR410506 **Set No. 3**

IV B.Tech I Semester Supplimentary Examinations, November 2008
FAULT TOLERANT SYSTEMS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Distinguish between failures, and faults ? Explain. [2+2]
   (b) Explain the different modeling schemes of faults that generally come across in digital circuits. [3 × 2]
   (c) Explain the following terms with respect to digital circuits with suitable examples.
      i. Fault diagnosis.
      ii. Fault detection test set.
      iii. Test vector generation. [3 × 2]

2. (a) A circuit realizes the function.
   Z=$\overline{X_1}$ X_4+$\overline{X_2}$ X_3+$X_1\overline{X_4}$
   Using Boolean Difference method find the test vectors for SA0, SA1 faults on all input lines of the circuit.
   (b) What are the different properties of Boolean differences? Explain. [5+5+6]

3. (a) Construct a seven-bit error correcting code to represent the decimal digit by augmenting the Excess-3 code and by using add-1 parity check.
   (b) Design a redundant circuit for $f = a \oplus b$ [9+7]

4. (a) What is the goal of "pluibus" system used in ARPA network. Explain its working.
   (b) What is ment by fail soft operation? What should a system have to achieve the capability of fail soft operation. [4+4+4+4]

5. (a) What is the need for self checking circuits
   (b) Design a totally self checking checker by using reddy's partition method for 2out of 5 code. [6+10]

6. (a) Explain the general appraoch to the design of totally self-checking PLAs.
   (b) Explain why self-checking machines are essential in digital system. [10+6]

7. (a) What are the draw backs of Reed-Muller expansion Technique.
   (b) What is an unate function?
   (c) Give the design procedure for a completely fault locatable networks for unate function. [6+4+6]

8. (a) What is meant by built in test of VLSI? Explain.
   (b) Discuss the crosscheck approach to incorporate test circuitry into the basic cells used in implement VLSI design. [8+8]

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Code No: RR410506 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define the term Reliability of a system. Derive a relation for the R(t) in terms of constant failure rate λ. [3+5]
   (b) What is meant by Mean time between failures? How is it useful in system usage. Derive the expression of MTBF. [2+3+3]

2. For the circuit shown as in figure 2 , derive

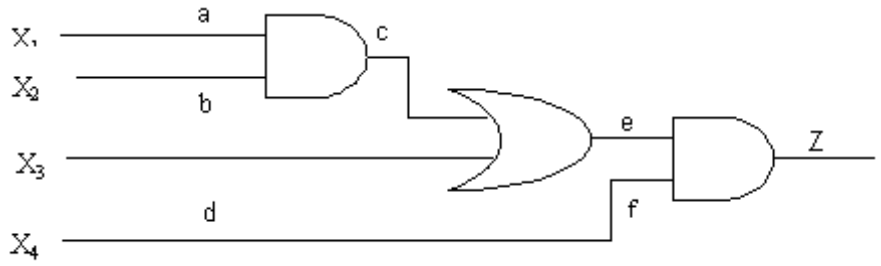

Figure 2

   (a) minimal complete fixed scheduled fault detection experiment.
   (b) minimal complete fixed scheduled fault location experiment. [8+8]

3. (a) Construct a seven-bit error correcting code to represent the decimal digit by augmenting the Excess-3 code and by using add-1 parity check.
   (b) Design a redundant circuit for $f = a \oplus b$ [9+7]

4. (a) Explain in detail the practicle fault Tolerant space shuttle computer complex system.
   (b) What are the different ways to have software redundancy. [8+8]

5. (a) What is the need for self checking circuits
   (b) Design a totally self checking checker by using reddy's partition method for 2out of 5 code. [6+10]

6. (a) Explain the advantages of PLA and how it is used as totally self-checking circuit.
   (b) For the given 4 input, 4 output function design a totally self checking checker circuit using PLAs. [6+10]
   f_1 (A,B,C,D) = $\sum$ (0,2,3,7,8,10,12,13,15)

f_2(A,B,C,D) = $\sum$ (0,2,3,4,9,12,13,15)
f_3(A,B,C,D) = $\sum$ (0,1,2,4,8,9,10,14)
f_4(A,B,C,D) = $\sum$ (0,1,2,4,5,6,8,11,14).

7. (a) What are the goals of a design for testability?
   (b) What are the different DET methods available? Explain at least two such techniques. [6+4+6]

8. Explain observability enhancement with neat diagram with suitable examples. [4+2+10]

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