Code No: RR220501 **Set No. 1**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information Technology, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe all optional PCI signal lines with designation and type. [16]
2. (a) Find the output binary number after performing the arithmatic operation using 1's complement representation.
   i. 111.01 + 10.111
   ii. 110.11 - 111.01
   (b) Explain steps involved in the addition of numbers using 2's complement notation. [10+6]
3. (a) Explain various control and status registers.
   (b) Compare register organizations of 8086 with MC68000 processors [8+8]
4. Elaborate on different types of registers in a register organization [16]
5. (a) What are the memory management requirements.
   (b) Elaborate on address translation in virtual memories [8+8]
6. Discuss about data organization and formatting of magnetic disk in detail [16]
7. (a) Discuss about wilke's microprogrammed control unit
   (b) Explain the organization of control memory [8+8]
8. (a) Explain different types of parallel processors.
   (b) What do you mean by compound instruction? Give examples
   (c) Elaborate on registers of the IBM3090 vector facility. [4+6+6]

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Code No: RR220501 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw and explain the timing of read operation in both synchronous and asynchronous timing.
   (b) Discuss various data transfer types supported by buses [8+8]
2. (a) Explain about booth coding
   (b) Find the booth coded numbers of the following binary numbers
      i. 01101111101
      ii. 000111110110 [8+8]
3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]
4. (a) Explain about the machine state register.
   (b) Discuss about the sequence of steps that occurs when an interrupt occurs [6+10]
5. (a) Explain the purpose of address translation. Give a general block diagram of it.
   (b) Differentiate between segment table and page table. [10+6]
6. Discuss the major functions and requirements for an I/O module. [16]
7. (a) Explain about microinstruction format of TI 8800
   (b) Explain about ALU control fields of IBM 3033 microinstruction. [8+8]
8. (a) Differentiate between two-stage and four-stage pipelines
   (b) Discuss the demerits of pipelined processing. [10+6]

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Code No: RR220501 **Set No. 3**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate between traditional and high performance bus architectures
   (b) List the key elements of bus design. [8+8]
2. Discuss about
   (a) Weighted codes
   (b) Self - complementing codes
   (c) Cyclic codes [5+5+6]
3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]
4. (a) List and describe integer arithmetic and logical instructions of Motorola 88000
   (b) Discuss about functioning of Motorola 88000 instruction unit pipeline. [8+8]
5. A block-set-associative Cache consists of a total of 64 blocks divided into four-block sets. The main memory contains 4096 blocks each consisting of 128 words
   (a) How many bits are there in main memory address?
   (b) How many bits are there in each of the TAG, SET, and WORD fields? [6+10]
6. Discuss about data organization and formatting of magnetic disk in detail [16]
7. (a) How the address of next microinstruction is known while executing a micro program.
   (b) Discuss about branch control logic in microinstruction sequencing with variable address format. [6+10]
8. (a) Differentiate between two-stage and four-stage pipelines
   (b) Discuss the demerits of pipelined processing. [10+6]

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Code No: RR220501 **Set No. 4**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
COMPUTER ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the generic structure of IAS computer in detail with the help of a block diagram. [16]
2. Write an algorithm to substract binary numbers represented in normalized floating point mode with base 2 for exponent [16]
3. (a) Discuss about power PC data types
   (b) Explain numerical data formats for Pentium floating point unit. [6+10]
4. (a) List various R3000 pipeline stages. Also explain the function of each.
   (b) List and describe all shift and multiply/divide instructions of MIPS R-Series processors. [8+8]
5. A block-set-associative Cache consists of a total of 64 blocks divided into four-block sets. The main memory contains 4096 blocks each consisting of 128 words
   (a) How many bits are there in main memory address?
   (b) How many bits are there in each of the TAG, SET, and WORD fields? [6+10]
6. (a) How would CPU handles multiple devices. Explain with different techniques available
   (b) Discuss the characteristics of Intel 8259A interrupt controller. [8+8]
7. (a) Explain the principles and working of dot matrix printers.
   (b) Differentiate between different types of printers. [8+8]
8. (a) Explain about directory protocols.
   (b) Draw and explain the state diagram for MESI protocol. [6+10]

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