

III B.Tech II Semester Supplementary Examinations, Apr/May 2008
MICROPROCESSORS AND INTERFACING
(Common to Electrical & Electronic Engineering, Electronics &
Communication Engineering, Electronics & Instrumentation Engineering,
Bio-Medical Engineering, Electronics & Control Engineering and Electronics
& Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. Discuss the general functions of all general-purpose registers of 8086? Explain the special function of each register and instruction support for these functions. [16]
2. Develop an 8086 assembly language program that reads a key from the keyboard and converts it to uppercase before displaying it. The program needs to terminate on typing the 'Ctrl + C' key combination. [16]
3. (a) What is the purpose of ALE, BHE, DT/\overline{R} and \overline{DEN} pins of 8086? Show their timing in the system bus cycle of 8086?
(b) Show the complete design to generate system address, data and control buses using the above pins, latches and transceivers. [8+8]
4. Explain why 8255 ports are divided into two groups? Discuss how these groups are controlled in different modes of operation? Explain different control signals and their associated pins for bi-directional I/O mode of operation? [4+6+6]
5. Interface 8251 with 8086 at address 40H. Initialize it in asynchronous transmit mode, with 7 bit character size, baud rate factor 16, one start bit, one stop bit, even parity enable. Further transmit a message "BEST OF LUCK" in ASCII from to a modem? [16]
6. (a) Discuss the sequence of operations performed in the interrupt acknowledge cycle?
(b) What is the difference between RET and IRET? Discuss the result, if RET instruction is placed at the end of the interrupt service routine?
(c) What is the vector address of type 50H interrupt? [6+6+4]
7. In a home PC with 8088 processor, SRAM is provided from 00000H and EPROM ends with the address of FFFFFH. The capacity of SRAM is 256KB and that of EPROM is 32KB. All the chips are of size 32KB. Give the address map for individual chip and design the complete memory interface? [16]
8. Interface two 8255's to 8051 with starting address of 0FFF0H? Show the hardware design? Write the instruction sequence to initialize all ports of 8255s as input ports in mode 0. [16]

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1. (a) Compare 8 bit processors and 16 bit processors from the architectural view.
(b) Explain Overflow condition with 8 bit signed data. Generate Overflow flag using other flags of 8086? [6+10]
2. (a) Explain the coding template of 8086 instruction? Discuss the coding template of MOV instruction?
(b) Discuss the importance of procedures in assembly language programming? [9+7]
3. Describe the function of the following pins and their use in 8086 based system.
(a) DEN
(b) \overline{LOCK}
(c) \overline{TEST}
(d) READY [4 x 4 = 16]
4. Interface an 8-bit DAC to 8255 with an address map of 0100H to 0103H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence for the following?
(a) For generating a square wave with a peak to peak voltage of 2V and the frequency will be selected from memory location 'FREQ'. [6+10]
(b) For generating a triangular wave with a maximum voltage of +4V and a minimum of -2V.
5. (a) Draw the flowchart showing how synchronous serial data can be sent from a port line using software routine?
(b) Draw the block diagram of 8237 and explain each block. [8+8]
6. (a) Which interrupt type is associated with NMI? Mention its vector address?
(b) What is the purpose of IF flag in handling the interrupts?
(c) Which interrupt type is associated with TF flag? What is the vector address? Explain the use of this interrupt? [5+5+6]

7. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]
8. (a) Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?
- i. SCON
 - ii. TCON [4x2=8]
- (b) Discuss the following signal descriptions?
- i. ALE/PROG
 - ii. \overline{EA}/V_{pp}
 - iii. \overline{PSEN}
 - iv. RXD [2x4=8]

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1. The register contents of 8086 is given below.
CS=5000H, DS=8000H, SS=9000H, ES=7000H, SI=1000H, DI=2000H, BP=0008H,
SP=0002H, AX=0000H, BX=5200H, CX=8000H, DX=2800H
Calculate the effective address and physical address of the following instructions.
 - (a) MOV AX, [BP+BX-24D]
 - (b) ADD AX, ES:[SI]
 - (c) PUSH CX
 - (d) SUB AX, [DI]
 - (e) MOVSB
 - (f) CMP AX, [DI]
 - (g) ADD DX, [DI+8D]
 - (h) MUL AX, [SI+2D] [16]

2.
 - (a) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two-digit Hex number?
 - (b) What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions. [9+7]

3.
 - (a) Explain how an 8086 enters into Wait State? How many wait states can be inserted in a machine cycle?
 - (b) What is the difference between system bus cycle and bus idle cycle? Draw the timing diagram of bus idle cycle? [6+10]

4.
 - (a) With neat layout, explain how a microprocessor can be used for data acquisition system using A/D converters and D/A converters?
 - (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [10+6]

5.
 - (a) Explain demand transfer mode and block transfer mode of 8237?
 - (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?

- (c) Explain how memory to memory transfer is performed with 8237? [5+6+5]
6. (a) How many initialization command words are required for a single 8259 in an 8086 based system? Explain their format?
(b) Under what conditions type 0 interrupt is initiated? List out the instructions that may cause type 0 interrupt? [10+6]
7. (a) With a sketch explain 74LS138 decoder and its use?
(b) What is a memory module? Draw the block diagram of SDRAM module and explain each block?
(c) Generate even and odd address memory bank select lines for 8086 processor? [6+6+4]
8. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
(a) IP
(b) TMOD
(c) TCON
(d) SCON [4x4=16]

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1. It is necessary to check whether the word stored in location 3000H:2000H is zero or not. Show all possible ways of testing the above condition using different addressing modes and store 0FFH if the condition is satisfied in location 3000H:2002H. Otherwise store 00H. [16]
2. (a) Explain in detail the coding template for 8086 MOV instruction? [8]
(b) Write briefly about
 - i. PUBLIC directive
 - ii. EXTERN directive [4+4]
3. (a) Explain how an 8086 enters into Wait State? How many wait states can be inserted in a machine cycle?
(b) What is the difference between system bus cycle and bus idle cycle? Draw the timing diagram of bus idle cycle? [6+10]
4. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
 - (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
 - (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
 - (c) Port A in mode 0, port C upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
 - (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]
5. (a) Explain demand transfer mode and block transfer mode of 8237?
(b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
(c) Explain how memory to memory transfer is performed with 8237? [5+6+5]
6. (a) Draw the block diagram of 8259 and explain each block? Discuss the salient features of 8259?

- (b) What is the address map of interrupt address vector table? How many interrupts that this table can serve? [11+5]
7. A target system based on 8088 processor uses less amount of SRAM. The programs are stored in EPROM that starts from F0000H ends with the address of FFFFFH. The capacity of SRAM is 8KB interfaced at address 00000H. The chip size is 8KB for EPROM and SRAM. Show the complete memory interface? [16]
8. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
- (a) IP
 - (b) TMOD
 - (c) TCON
 - (d) SCON
- [4x4=16]
