C. ABDUL HAKEEM COLLEGE OF ENGG & TECH

DEPARTMENT OF COMPUTER APPLICATIONS

QUESTION BANK

SUBJECT: COMPUTER ORGANIZATION **CODE :MC7101**

BRANCH: I M.C.A **SEM : I**

PART-A (2 MARKS)

UNIT I

1. What are number systems?

In mathematics, a 'number system' is a set of numbers, together with one or more operations, such as addition or multiplication.

Examples of number systems include: natural numbers, integers, rational numbers, algebraic numbers, real numbers, complex numbers, p-adic numbers, surreal numbers, and hyperreal numbers

2. Convert decimal 41 to binary.

2	41	
2	20 – 1	
2	10 – 0	
2	5 -- 0	
2	2 -- 1	
	1 -- 0	

Ans. $(41)_{10} = (101001)_2$

3. **Convert decimal $(153.513)_{10}$ to octal**.

8	153	.513 * 8 = 4
8	19 – 1	.104 * 8 = 0
	2 – 3	. 832 * 8 = 6
		. 656 * 8 = 5
		. 248 * 8 = 1

Ans:

$(153.513)_{10} = (231.40651)_8$

4. **Why NAND & NOR are called universal gates?**

Basic logic gates are AND, OR & NOT. Since any basic logic gates can be constructed using NAND & NOR gates, they are called as universal gates.

5. Give the advantages & disadvantages of of K-map.

Advantage: It is used to simplify Boolean function of upto 6 variables.

DisAdvantage: i) Boolean function simplification is complicated when no. of variables exceeds 6.
ii) There is no systematic approach is used in K-map in BF simplification.

6. Write the purpose of Boolean algebra.

1. Express in algebraic form a truth table relationship between binary variables
2. Express in algebraic from the input-output relationship of logic diagrams
3. Find simpler circuits for the same function

7. **Simplify the following Boolean functions to a minimum number of literals**: a) (x+y) (x+y')
b) y(wz' + wz) + xy

a) (x+y)(x+y') = xx+xy'+xy+yy'
= x+x(y'+y)+yy'

=x+x+0

= x

b) y(wz' + wz) + xy = y(w(z+z'))+xy

= yw+xy

8. **What is K-Map?**

A map method provides a simple, straightforward procedure for simplifying boolean expressions in pictorial representations. This map method is also known as the K-map or Karnaugh map

9. **Convert the decimal no 250.5 to base 8**

8	250
8	31 – 2
8	3 -7

Ans: $(250.5)_{10} = (372_{)8}$

10. **Convert the following nos to decimal**:

i) $(1001001.011)_2$

$1001001 = (1* 2^{0}) + 0 + 0 + (1 * 2^{3}) + 0 + 0 + (1* 2^{6}) = 73$

$0.011 = 0 * 2^{-1} + 1 * 2^{-2} + 1* 2^{-3} = 0.375$

$= 73.375$

11. **Write the complement for the following Boolean function using the principle of duality or de morgan's law.**
F= (x+y) * (x ' + xy)
Ans: F = (x' y') + (x * x'y')

12**. Convert the following to its equivalent hexadecimal number.**
1001 0001 1111 0000 = 9 1 F 0
0010 1000 1010 0001 = 2 8 A 1

13. **Give the demorgan's law with its equations**
(a+b)' = a' . b'
(a.b)' = a' + b'

14.**What is truth table?**
The relationship between a function and it's binary variables can be represented in a truth table.

15. **Define Logic circuits**
The manipulation of binary infromation is done by logic circuits is called gates or Logic gates

16. **List out the names of logic gates**
AND, OR, Inverter, Buffer, NAND, NOR, XOR, XNOR

17. **List the differences between AND & NAND gates.**
AND gates gives output is 1 if input A and input B are both equal to 1 otherwise the output is 0. NAND gate is a complement of AND function

18. **What is computer organization?**
Computer organization is concerned with the way the hardware components operate and the way they are concerned together to form the computer system.

19. **Define signal.**
Binary information is represented in digital computers by physical quantities called signals

20. **What is combinational circuits?**

A combinational circuit is a connected arrangement of logic gates with a set of inputs and outputs.

21.**What is 9's and 10's complement?**

Given a number N in base r having n digits, the (r-1)'s complement of N is defined as (r^n-1)-N.F or decimal number r=10 and r-1=9, so the 9's complement of N is (10^n-1)-N.

22. **What are the largest positive number and largest negative number which can be represented**

in an 8-bit register, using the sign-magnitude method of representation?

Largest Positive number: +127 (0111 1111)
Largest Negative number: -127 (1111 1111)

23. **How many positive binary numbers can be represented in a byte using the sign-magnitude notation?**

If 0 is counted as a positive integer, the numbers range from 0000 0000 to 0111 1111 which is 0 to 127 which is 128 different integers

24**. If R = -11 and S = +21, use 2's complement form to find R - S.**

Ans: -11 - (+21) is the same as -11 + (-21).

	Decimal Subtraction as Addition	2's Complement Addition
Minuend	-11	1111 0101
Subtrahend	+ -21	+ 1110 1011
Difference	-32	1 1110 0000 Ignore the final carry. The answer is 1110 0000 which is -32 in decimal.

25**. Using a word of 3 bits, list all possible signed binary numbers and their decimal equivalents**

that are represented in two's complement.

Signed binary numbers are: 100, 101, 110, and 111

The corresponding 2's complements are 100, 011, 010, 001 the respective decimal equivalents are 4, 3, 2, 1

UNIT II

1. **What is Encoder?**
   An encoder is a digital circuit that performs the inverse operation of a decoder.
   an encoder has 2^n input lines and n output lines
2. **What is Decoder?**
   A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs
3. **Differentiate between encoder and decoder.**
   Encoder is the reverse of a decoder. In a decoder it has n input lines and 2^n output lines, but in an encoder it has 2^n input lines and n output lines.
4. **Differentiate combinational and sequential circuits.**
   A combinational circuit is the binary relationship between the n input and the m output variables combinations. A sequential circuit is an interconnection of flip-flops and gates, but when used with overall circuit is called sequential circuit.

5. **What is a flip flop?**

   A flip-flop is a binary cell capable of storing one bit binary information .It has two outputs, one for normal value and one for the complement value of the bit stored in it.

6. **Define mantissa and exponent**.

   The floating-point representation of a number has two parts. The first part represents a signed, fixed-point number called the mantissa. The second part designates the position of the decimal point and is called the exponent.

7. **Differentiate between half adder and full adder**.

   A combinational circuit that performs the arithmetic addition of two bits is called a half-adder. One that performs the addition of three bits is called a full-adder.

8. **Write down the truth table for full adder.**

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

9. **What is RISC?**

RISC nothing but Reduced Instruction Set Computer in which the instruction set chosen for a particular computer determines the way that machine language programs are constructed.

10 **What is CISC?**

CISC commonly known as Complex Instruction Set Computer with a

large number of instructions

11. **List out the types of flip-flop**

The various types of flip-flops are : 1. J-K flip-flop, 2. D Flip flop, 3. RS flip flop

12. **What is NAND gate decoder?**

Some decoders are constructed with NAND gate instead of AND gate is called NAND gate

decoder

13. **Define multiplexer?**

A multiplexer is a combinational circuit that receives binary information from 2^n input data lines and directs it to a single output line.

14. **Compare encoder and decoder.**

An encoder is a digital circuit performs the inverse operation of a decoder. An encoder has 2^n input lines and n output lines.

A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.

15. **Define register and register load.**

A register consists of groups of flip-flop capable of storing one bit of information.

The transfer of new information into a register is referred to as register load.

16.**What is a shift register?**

A register capable of shifting its binary information in one or both directions is called a shift

register.

17. **What is a binary counter?**

A register that goes through a predetermined sequence of states upon the application of input

pulses is called a binary counter.

18. **Differentiate between register transfer and register transfer language?**

Information transfer from one register to another is designated in symbolic form by means of a replacement operator. This is called as register transfer.

The symbolic notation used to describe the micro operation transfers among registers is called a register transfer language.

19. **Define bus.**

A bus structure consists of a set of common lines, one for each bit of a register, through which binary information is transferred one at a time.

20. **Differentiate between binary adder and binary incrementer**.

The digital circuit that generates the arithmetic sum of two binary numbers of any length is called a binary adder. The increment micro operation adds one to a number in a register. This micro operation is easily implemented with a binary counter.

21. **What is logical shift, circular shift and selective clear?**

A logical shift is one that transfers 0 through the serial input. The circular shift circulates the

bits of the register around the two ends without loss of information. The selective clear

operation clears to 0 the bits in A only where there are corresponding 1.

22. **Differentiate between selective complement and selective set**

The selective-complement operation complements bits in register A where there are corresponding 1. The selective set operation sets to 1 the bits in register A where there are corresponding 1’s in the register.

23. **What do you mean by arithmetic logic shift unit?**

Instead of having individual registers performing the micro operations directly, computer systems employ a number of storage registers connected to a common optional unit called an arithmetic logic unit.

24. **What is the use of location counter?**

To keep track of the location of instructions, the assembler uses a memory pointer called a location counter.

25. **Define pointer counter.**

The pointer points to the address of the current operand and counter counts the number of times that the program loop is executed.

UNIT III

1. **Differentiate between instruction code and operation code?**
   An instruction code is a group of bits that instruct the computer to perform a specific operation

   An operation code is a group of bits that define such operations as add, multiply, shift, and complement.

2. **What do you mean by an effective address?**
   The effective address is the address of the operand in a computation-type instruction or the target address in a branch-type instruction.

3. **What are the basic computer instruction formats**?
   The three basic computer instruction formats are

   a.Memory-reference instruction, **b**.Register-reference instruction, & **c**.input- output instruction.

4. **What is an IR?**
   The instruction register(IR) holds the instruction that is currently being executed. Its output is available to the control circuits, which generate the timing signals that controls the various processing elements involved in executing the instruction.

5. **Differentiate between hardwired control and micro programmed control.**
   In hardwired organization, the control logic is implemented with gates, flip-flops, decoders, and other digital circuits.

   In micro programmed control any required changes or modifications can be done by updating the microprogram in control memory.

6. **What are the different phases of an instruction cycle?**
   a.Fetch an instruction from memory , b. Decode the instruction, c.Read the effective address from memory if the instruction has an indirect address, d. Execute the instruction.

7. **List the four types of operations**.
   a.Data transfers between the memory and the processor registers, b.ALU operations on data, c.Program sequencing and control,d. I/O transfers.

8. **What are the types of instruction formats?**

   Three –address instruction, Two–address instruction, One–address instruction, zero address instruction

9. **How many references to memory are needed for indirect address instruction to bring the operand**

into a processor register ?

Two references are needed for indirect address instruction to bring the operand into a processor

Register.

10. **Give example for One–address instruction**

ADD A, SUB B, HLT,

11**. Define pseudo instruction**.

A pseudo instruction is not a machine direction but rather an instruction to the assembler giving information about some phase of the translation.

12. **Define address symbol table.**

The translation process can be simplified if we scan the entire symbolic program twice. No translation is done during the first scan.

13**. What is a subroutine ?**

A set of common instructions that can be used in a program many times is called a subroutine.

14. **What is meant by program interrupt?**

The running time of input and output programs is made up primarily of the time spent by the computer in waiting for the external device to set its flag.

15**. Explain PC(program counter).**

The PC points to the address of the instruction to be executed next.

16**. Define program loops.**

A program loop is a sequence of instructions that are executed many times with each time with a different set of data.

17**. List the four commonly used flags.**

N(negative) →set to 1 if the result is negative ; otherwise, cleared to 0, V(overflow →set to 1 if

arithmetic overflow occurs; otherwise, cleared to 0, Z(zero) → set to 1 if the result is 0; otherwise,

cleared to 0, C(carry) →set to 1 if the carry-out results from the operation; otherwise, cleared to 0.

18. **What is the use of location counter ?**

To keep track of the location of instructions, the assembler uses a memory word called a location counter.

19. **List the micro operations for the fetch and decode phase.**

T0: AR←PC
T1: IR← M[AR], PC ←PC+1
T2: D0……D7 ← DECODE IR[I2-I4]
I ← IR[15]
AR← IR[0….11]

20. **List the major characteristics of a RISC processor.**

Relatively few instructions, Relatively few addressing modes, Memory access limited to load and store instructions, All operations done within the registers of the CPU, Fixed-length, easily decoded instruction format, Single-cycle instruction execution, Hardwired rather rhan microprogrammed control

21 **List the characteristics of a CISC processor.**

A large number of instructions, Some instructions that perform specialized tasks and are used infrequently, A large variety of addressing modes – typically from 5 to 20 different modes, Variable-length instruction formats, Instructions that manipulate operands in memory

UNIT IV

1. **Write down the steps required to execute an instruction.**
   - Fetch the contents of the memory location pointed to by the PC. The contents of this location are interpreted as an instruction to be executed. Hence, they are loaded into the IR.

     IR < [[PC]]

   - Assuming that the memory is byte addressable, increment the contents of the PC by 4, i.e PC < [PC]+4
   - Carry out the actions specified by the instruction in the IR**.**

2. **What is a data path?**

   The registers, the ALU, and the interconnecting bus are collectively reffered to as the datapath.

3. **Give the steps needed to execute the following instruction: MOVE (R1),R2**
   - MAR < [R1]
   - Start a read operation on the memory bus
   - Wait for the MFC response from the memory
   - Load MDR from the memory bus
   - R2 < [MDR]

4. **Give the control sequence for storing a word in memory**.

   - $R1_{out}$, MAR_{in}
   - $R2_{out}$, MDR_{in}, Write
   - MDR_{out}, WMFC

5. **What is a control word?**
   A control word is a word whose individual bits represent the various control signals.

6. **Define microroutine.**
   A sequence of CWs(control word) corresponding to the control sequence of a machine instruction constitute the microroutine for that instruction

8. **Define microinstructions**.

   The individual control words in this microroutine are referred to as microinstructions.

9. **What is a control store?**

   The microroutines for all instructions in the instruction set of a computer are stored in a special memory called the control store. The control unit can generate the control signals for any instruction by sequentially reading the CWs of the corresponding microroutine from the control store.

10. Define vertical organization

Highly encoded schemes that use compact codes to specify only a small number of control functions in each microinstruction are referred to as a vertical organization.

11. What is horizontal organization?

Minimally encoded scheme in which many resources can be controlled with a single microinstruction , is called a horizontal organization.

12. Define emulation'

Suppose we add to the instruction repertoire of a given computer, M1, an entirely new set of instructions that is in fact the instruction set of a different computer, M2. Programs written in the machine language of M2 can then be run on computer M1, that is, M1 emulates M2.

13. **Define pipeline**.

It is a effective way of organizing concurrent activity in a computer system is called pipeline

14. What is a hazard?

Any condition that causes the pipeline to stall is called a hazard.

15. What is data hazard?

Data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline. As a result some operation has to be delayed , and the pipeline stalls.

16. What is control or instruction hazard?

The pipeline may also be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control or instruction hazards.

17. What is structural hazard?

This is the situation occurs when two instructions require the use of a given hardware at the same time . This type of hazard may arise in memory access. One instruction may need to access memory as part of the execute or write stage while another instruction can is being fetched. If instructions and data reside in the same cache unit , only one instruction can proceed and the other instruction is delayed.

18. Explain superscalar processor.

It is an approach to equip the processor with multiple processing units to handle several instructions

in parallel in each processing stage. With this arrangement , several instructions start execution in the

same clock cycle, and the processor is said to use multiple-issue. Such processors are capable of

achieving an instruction execution throughput of more than one instruction per cycle. They are

known as superscalar processor.

19. Explain Speculative execution.

Speculative execution means that the instructions are executed before the processor is certain that they are in the corrective execution sequence.Hence care must be taken that no processor registers or memory locations are updated until it is confirmed that these instructions should indeed be executed. If the branch decision indicates otherwise, the instructions and all their associated data in the execution units must be purged , and the correct instructions fetched and executed.

20. What are the two states of dynamic branch prediction algorithm?

LT : Branch is likely to be taken , LNT : Branch is likely not to be taken

21**. List the four states of strongly likely to be taken**

ST : strongly likely to be taken, LT : Likely to be taken, LNT : Likely not to be taken

SNT : Strongly likely not to be taken

21. What are the various ways of maintaining the state information used in dynamic branch prediction algorithm?

The various ways of maintaining the state information used in dynamic branch prediction algorithm

are: Look-up table, Store the history bits as a tag associated with branch instructions in the instruction

cache.

22. What are the various approaches of branch prediction?

The various approaches of branch prediction : Static branch prediction, Dynamic branch prediction

23. Distinguish between static branch prediction and dynamic branch prediction.

a. **Static branch prediction :** The branch prediction decision is always the same every time a given instruction is executed.
b. **Dynamic branch prediction :** The branch prediction decision may change depending on execution history.

UNIT V

1. **What is memory-mapped I/O?**
   In memory-mapped I/O, I/O devices and the memory share the same address space.

2. **What are the various mechanisms for implementing I/O operations?**
   The various mechanisms for implementing I/O operations are:

   - Program-controlled I/O, Interrupted I/O, Direct memory access

3. **What do you mean by program-controlled I/O?**
   In program-controlled I/O, the processor repeatedly checks a status flag to achieve the required synchronization between the processor and an I/O device. That is the processor polls the device.

4. **What is an interrupt?**
   The signal given by the I/O devices to alert the processor, whenever they need the service from the processor .

5. **What is ISR(Interrupt Service Routine)?**

   The routine executed in response to an interrupt request is called the interrupt service routine.

6. **What is DMA?**
   It is a technique used for high-speed I/O devices. It involves having the device interface transfer data directly to or from the memory, without continuous involvement by the processor.

7. **What is DMA controller?**
   DMA transfers are performed by a control circuit that is part of the I/O device interface. This circuit is referred as DMA controller.

8. **Mention the registers used in DMA interface.**
   The registers used in DMA interface are Status and control register, Starting address register and Word count register

9. **What is a bus master?**
   The device that is allowed to initiate data transfers on the bus at any given time is called the bus master. When the current bus master relinquishes control of the bus, another device acquire this status.

10. **What do you mean by bus arbitration?**
    It is the process by which the next device to become the bus master is selected and bus mastership is transferred to it.

11. What are the two approaches to bus arbitration?

The two approaches to bus arbitration are Centralized bus arbitration and Distributed bus arbitration

12. Explain centralized bus arbitration.

In centralized bus arbitration, a single bus arbiter performs the required arbitration.

13. Explain distributed bus arbitration

In distributed bus arbitration, all devices participation in the selection of the next bus master.

14. Explain Daisy chaining.

This method involves 3 control signals namely BUS REQUEST , BUS GRANT & BUS BUSY. All the bus units are connected to the BUS REQUEST line. When activated it merely serves to indicate that one or those units are requesting the use of the bus. The controller responds to a bus request signal only if BUS BUSY is inactive on receiving the BUS GRANT signal . A requesting unit enables its physical buses connections and activates BUS BUSY for the duration of its new bus activity.

15. Explain polling method.

The polling method replaces the BUS GRANT line which is seen in daisy chain instead it has a set of poll count lines that are connected to all units on the bus.

It is a process of determining the source with higher priority through software means.

16. What is the advantage of polling over daisy chaining?

In polling a failure in one unit need not affect the other units.

17. What is the disadvantage of synchronous communication?

The drawback of synchronous communication is that the data transfer rates are slow, some devices may not be able to communicate at their maximum rate.

18. What is meant by cycle stealing?

This is a technique which allows the DMA controller to use the system bus transfer one data word and after which it must return control of the bus to the CPU. The cycle stealing reduces the maximum IO transfer rate but it also reduces the interference by the DMA controller in the CPU's memory access.It is used in case of low speed devices. Here there is a steal of memory cycle takes place.

19. **Explain the operations of DMA**.

DMA eliminates the role of CPU and increased the speed of IO operations.

Signals on the special control lines cause the CPU to suspend current activities at necessary points and attend to DMA or Interrupt request. This eliminates the CPU to execute routines to determine the status of IO devices. The DMA also allows IO data

transfers to take place without the execution of IO instructions by the CPU. DMA request by an IO devices only requires the CPU grant control to memory(system) to the requesting system.

20. **Explain the functions of a bus master**.
The device that is allowed to initiate data transfers on the bus at any given time is called the bus master.

21. What do you mean by a bus cycle?
In a synchronous bus, all devices derive timing information from a common clock line. Equally spaced pulses on this line define equal time intervals. In the simplest form of a synchronous bus, each of these intervals constitutes a bus cycle during which one data transfer takes place.

21. **Differentiate asynchronous and synchronous data transfer?**

In synchronous transmission the two units share a common clock frequency and bits are transmitted continuously.

In asynchronous transmission terminals employs a special bits that are inserted at both ends of the character code.

22. **Define Priority interrupt.**

A priority interrupt is a system that establishes a priority over the various sources to determine which condition is to be served first when two or more requests arrive simultaneously.

23. **Differentiate between vectored interrupt and non –vectored interrupt**

In a vectored interrupt, the source that interrupts supplies the branch information to the computer. This information is called the interrupt vector.

In a non vectored interrupt, the branch address is assigned to a fixed location in memory.

25. **What do you mean by a initiator and a target?**

At any given time one device is the bus master. It has right to initiate data transfers by issuing read and write commands. A master is called an initiator in PCI terminology. This is either a processor or a DMA controller. The addressed device that responds to read and write commands is called a target.

26. **Define cache memory.**

If the active portions of the program and data are placed in a fast small memory, the average memory access time can be reduced, thus reducing the total executing time of the program. Such a fast small memory is referred to as a cache memory.

27. **What is meant by locality of reference?**

In locality of reference typical computer program flows in a straight-line fashion with program loops and subroutine calls encountered frequently.

28. **Differentiate between SRAM and DRAM.**

Memories that are capable retaining their state as long as power is applied is known as static memories or SRAM.

Cells that do not retain their state indefinitely are called dynamic RAM. Here information is stored in the form of a charge on a capacitor. A DRAM is capable of storming information for only a few milli-seconds. The data stored is maintained by restoring the capacitor charge to its full value.

29. **Define virtual memory.**

Virtual memory is a concept that permit the user to construct programs as though a large memory space available equal to the totality of auxiliary memory.

30. **Define address space and memory space?**

The set of virtual address is called the address space, The set of physical address is called the memory space.

31. **What are the various methods used to determine cache locations?**

The various methods used to determine cache locations are Direct mapping, Associative mapping,

Set-associative mapping,

32. **Differentiate between RAM and ROM**.

Random Access Memory – RAM is a Read/Write memory, i.e. information can be written into it or read from it. A word stored can be accessed from RAM in a given amount of time. The access time is independent of the position of the word. RAM is used for storing application programs, storing intermediate results during program execution. RAM is normally volatile.

Read Only Memory (ROM) is a memory that is permanently programmed and can only be read. No information can be written into ROM. ROM is employed to store programs required permanently called the firmware. ROM is non-volatile.

16-MARKS

PART-B

UNIT-1

1. Define number systems. Explain about various number system and it's conversion.
2. Write a short note on various logic gates function with it's neat diagram
3. Simplify the Boolean function F together with the don't care conditions d in
   F(W,X,Y,Z) = ∑ (0,1,2,3,7,8,10) , D(W,X,Y,Z) = ∑ (5,6,11,15)
4. Design a code converter that converts a decimal digit from BCD to Excess- 3 code.
5. Implement the following using NOR gates.F = AC'+B'D+A'CD+ABCD
6. Using Demorgan's law show that (8+8=16)

   a) (A+B)'(A'+B')=0, b) A+A'B+A'B'=1
7. Simplify the following expressions using Boolean algebra (4x4=16)

   a) A+AB, b) AB+AB', c) A'BC+AC, d) A'B+ABC'+ABC
8. Write the différence between AND & NAND gates and also write the implementation concept of

   NAND gate
9. Explain about basic identities of boolean algebra
10. Write a note on following : (4x4=16)

    a) Boolean algebra, b) Truth table, c) EX-OR gate. D) Logic diagram

UNIT-2

1. Design a counter using JK flip flop for the sequence 0,1,2,4,5,6
2. i) Design half adder and full adder using only universal gates(10)

   ii) Explain the use of D flip flop

3. Design a sequential circuit with two flip flops and one input x. When x= 1 the state Of the flip flops does not change. When x = 0 the state sequence is 00, 01, 10 &11
4. Design a combinational circuit with 3 inputs and 6 outputs. The output binary number should be the square of the input binary number.
5. (a)Design a binary adder subtracted circuit (8)

   (b) Design a BCD subtractor circuit using 9's compliment method.

6. Construct 16×1 multiplexers with two 8×1 multiplexers and one 2×1 multiplexers. Using block diagrams for the three multiplexers and explain it.
7. Design a counter using D flip flops that counts the sequence 00, 01, 10,00,01,10. Draw the timing diagram for the Q signal of the flip flop used.
8. (a) Design a BCD to decimal decoder. (8)

   (b) What are the various types of shift operations? Give example for each type. Design a 4 bit circuit shifter for shifting the data left or right. (8)

9. Construct a 5-32 line decoder with 3-to 8 line decoders with enable and one 2- to -4 line decoder.
10. (a) Design a binary adder subtracted circuit (8)

    (b) Design a BCD subtractor circuit using 9's compliment method

UNIT-3

1. Derive an algorithm in flowchart form for add and subtract operations.
2. Explain booth algorithm for multiplication of signed 2's complement numbers.
3. Design an array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.
4. Derive an algorithm in flowchart form for multiplication of floating-point numbers.

5. Discuss in detail about RISC and CISC?
6. Explain instruction execution and straight-line sequencing
7. Explain ALU design
9. *Explain basic instruction types*
10. *Explain various addressing modes.*
11. *explain implementation of floating point operations*

UNIT-4

1. Explain single bus organization of the datapath inside a processor.
2. Explain multiple bus organization
3. Discuss about hardwired control.
4. Explain about microprogrammed control.
5. Discuss in detail about pipelining concepts.
6. Explain pipeline performance
7. Discuss in detail about data hazards.
8. Discuss in detail about instruction hazards
9. Give an account on branch prediction.
10. Explain superscalar operation

UNIT-5

1. Explain in detail about interrupts.
2. Discuss about DMA
3. Explain with example mapping techniques.
4. Explain in detail about asynchronous and synchronous bus
5. Discuss how memory blocks are placed in the cache.
6. Explain the following: Replacement algorithms, b. Interleaving, c. Hit rate and miss penalty
7. Explain about virtual memory
8. Discuss about a virtual-memory address translation method.
9. Write short notes on: Write buffer, Prefetching, Lookup-free cache, Memory hierarchy
10. Explain semiconductor RAM memories