BCA (T113): (Digital Electronics)

1. Complement of a variable is always its_____.
2. Determine the logic gate to implement the following terms--ABC, A+B+C?
3. What is parity generation ?
4. Add the following BCD numbers--- 1001 and 0100?
5. Equivalent Gray code representation of AC2H.?
6. A NAND gate becomes ___ gate when used with negative logic ?
7. Implement the logic equation Y = _ C' B A' + C' B A + CBA with a multiplexer.
8. Distributive law states that_____.
9. Represent standard SOP & POS form?
10. OR operation can be produced by _____gates.
11. _____is known as a universal gate as can be used to implement all Boolean expressions.
12. Simplify the expression AB + A(B + C) + B (B + C)?
13. a 3 variable karnaugh map has_____ cells.(eight cells)
14. On karnaugh map grouping of 0's produces_____(POS expression).
15. State distributive law?
16. State De Morgans theorem?
17. Give an example of SOP form?
18. According to assosiative law _____.[A(BC)=AB(C)]
19. A logic circuit with an output X=AB'C+AC' consist of _____ gates, _____gates and _____inverters.(two,one,two)
20. The OR operations can be produced with two_____gates or three_____gates.(NOR,NAND)
21. The AND operation can be produced with two_____gates.(NAND)
22. What is a decoder?(a digital circuit that converts coded informationinto a familiar or noncoded form)
23. Define demultiplexer?(a circuit that switches digital data from one input line to several output lines in a specified time sequence)
24. Difference between half adder and full adder?
25. A half adder is characterized by _____inputs and_____ outputs.(two,two)
26. A full adder is characterized by _____inputs and_____outputs.(three,two)
27. A 4 bit parallel adder can add _____4 bit binary numbers.(two)
28. Data selectors are basically same as _____.(multiplexers)
29. A multiplexer has _____data inputs,_____data outputs and selection inputs.(several,one)
30. What is 1's complement.
31. What is 2's complement.

32. Define Gray code with example.
33. What Karnaugh Map.How it represent.
34. Obtain the following operations using NAND gates.
    a) NOT   b) AND   c) OR
35. Obtain the following operations using NOR gates.
    a) NOT   b) AND   c) OR
36. For the logic expression

    $Y = A\ \bar{B}\ +\ \bar{A}\ B$

    Obtain the truth table and Name the operation performed.
37. Prove using De Morgan's theorems.

    $AB + CD = \overline{\bar{AB}.\ \ \bar{CD}}$
38. Prove using De Morgan's theorems.

    $\overline{\overline{(A+B)} + \overline{(C+D)}}$
39. Define De Morgan's theorems.
40. Verify the following gate with Truth Table.
    - OR,
    - AND
    - NOT
    - NAND
    - NOR
    - XOR
    - XNOR
41. What is a digital signal.
42. Differentiate between analog & digital signals.
43. Convert the binary number into octal number
    11011100.101010
44. Add the binary numbers
    1011 + 1101
    1010.1101 + 101.01
45. Subtraction the binary numbers
    1011 − 0110
    1110 − 1001
46. Find 1's complement of the numbers.
    a) 10100111   b) 01111
47. Find the 2's complement of the number
    01100100

48. Represent the following decimal numbers in the signed binary number system.
    +29   &   -29
49. Perform the subtraction using 2's complementary arithmetic
    11011 – 11001
50. Convert the BCD number to their decimal equivalent.
    0100 0011 1001
51. What is Excess-3 Code. and perform Excess –3 code of 14.
52. Convert the binary number into Gray code.
    110100
53. Convert the Gray code into binary number
    101110
54. Define ASCII Code.
55. Define EBCDIC Code.
56. What is a min term & max term.
57. What is the parity of the binary number 100110011.
58. Implement the Boolean expressions using minimum number of gates.
    $Y = ABC + \overline{ABC}$
59. Draw & explain:
    - binary half adder.
    - binary full adder.
    - binary half subtractor.
    - binary full subtractor
60. How can full adder be realized using two half adders
61. Show how to connect NAND gate to get an AND gate.
62. Perform 9's complement of 234.
63. Perform 10's complement of 567.
64. Explain tri-state logic.
65. Explain SOP form and POS form of logic expression.
66. What is a Karnaugh –map and what for it is used.
67. Convert $(1001110)_2$ to its octal equivalent.
68. Convert $(247.36)_8$ to equivalent hex number.
69. What is meant by parity of a digital word.
70. What is AND-OR realization.
71. What is OR-AND realization.
72. Represent the decimal numbers in 2's complement format.
    a) –5   b) –9
73. Find the two's complement of 10010010 & 11011000.
74. Perform subtraction using 2's complement method.
    0011.1001 – 0001.1110

75. Write the truth table of XNOR, NAND, NOR gate.
76. Prove using the Boolean algebraic theorems.

$A + \overline{A} \cdot B + \overline{A}\ \overline{B} = A + B$

$A.B + \overline{AB} + \overline{A}\ \overline{B} = A + B$

$ABC + A\ B\ \overline{C} + A\overline{BC} + \overline{ABC} = AB + BC + CA$

$AB + CD = (A+C)(A+D)(B+C)(B+D)$

$A\ (\overline{A} + C)(\overline{A}\ B + \overline{C}\ ) = 0$

$\overline{AB + BC + CA} = \overline{A}\ \overline{B} + \overline{B}\ \overline{C} + \overline{A}\ \overline{C}$

$\overline{\overline{AB} + A} + \overline{AB} = 0$

$\overline{A}\ \overline{B}\ C + \overline{A}\ B\ C + A\ \overline{B}\ C = \overline{A}\ C + A\ \overline{B}$

77. Simplify the Boolean expression

$A\ B\ C + A\ \overline{B}\ C + A\ \overline{B}\ C + A\ \overline{B}\ \overline{C} + A\overline{B}C + \overline{A}\ \overline{B}\ C$

$A\ B\ \overline{C}\ \overline{D}\ + A\ B\ \overline{C}D + A\ B\ C\overline{D} + A\ B\ C\ D$

78. Determine the decimal numbers represented by the following binary numbers:
    a) 110101   b) 1100.1011
79. Determine the binary numbers represented by the following decimal numbers:
    a) 37   b) 10.625
80. Convert the following decimal numbers to octal numbers
    a) 375   b) 27.125
81. Convert the following octal numbers into decimal numbers
    a) 237   b) 6327.4051
82. Convert the decimal numbers to hexadecimal.
    a) 375   b) 2047
83. Realize the following logic operations using only NAND gates
    a) NOT gate   b) AND gate   c) OR gate   d) NOR gate   e) XOR gate   f) XNOR gate
84. Realize the following logic operations using only NOR gates
    a) NOT gate   b) AND gate   c) OR gate   d) NAND gate   e) XOR gate   f) XNOR gate
85. Given the logic equation

$f = ABC + \overline{BC}D + \overline{A}BC$

Simplify using K-map. Realize f using NAND gates only.
86. Minimize the logic functions.

$f(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d\ (2,13)$

$f(A,B,C,D) = \prod M(1,2,3,8,9,10,11,14) + d\ (7,15)$

87. Find out the minimal expression for the switching function given below using the karnaugh map.

$\sum (A,B,C,D) = (0,1,4,5,6,7,12,14)$

88. Explain all gates (OR, AND, NOT, NOR, NAND, XOR , XNOR) with truth tables.

89. Given the logic equation

Y = (A + BC)(B + ꞁ A)

Design a circuit using gates to realize this function. Specify the number of gates required.

90. Minimize the functions and realize using minimum number of gates.

f = $\sum$m(0,3,5,6,9,10,12,15)

91. Minimize the functions and realize using minimum number of gates.

f = $\sum$m(0,1,2,3,11,12,14,15)

92. Add the binary numbers:

        0 1 1 0 1 0 1 0
        0 0 0 0 1 0 0 0
        1 0 0 0 0 0 0 1
        1 1 1 1 1 1 1 1
        ——————————————
        ——————————————

93. Convert decimal 1996 to an equivalent binary number.

94. Convert the binary number 11111001100 to its equivalent decimal number.

95. Convert the decimal number 274.1875 to its equivalent binary number.

96. Convert the Hexadecimal number CD42 to binary number.

97. Convert Hex numbers D2763 and B3D8 into decimal.

98. Convert decimal number to their equivalent octal numbers.

a) 4429.625   b) 11.9375

99. Write short notes on

a) Half Adder   b) Full Adder   c) Half Subtractor   d) Full Subtractor

100. Perform the following operations.

101. Convert (125)8 to binary b)(1C00)16 to decimal c) (8000)10 to hexadecimal

102. Convert (i) $532.65)_{10}$ = (? $)_{16}$ = (? $)_2$ (ii) $(ABCD)_{16}$ = (? $)_2$ = (? $)_8$

103. Convert (2AC5 . D $)_H$ to decimal , octal and binary

104. Use 2's complement to perform

a) $(1111 - 1101)_2$ b) $(10111 - 10011)_2$ c) $(1101 - 1001)_2$

105. Carry out subtraction using: I) 1's complement for ($101101 - 11001)_2$

106. Subtract 85 from 34 using 10's complement method

107. Perform the following operation. (765 $)_8$ − (637 $)_8$ + (725 $)_{16}$. Express the answer in octal form

108. Compute $(3B7)_H$ − $(854)_H$ using 16's complement method of subtraction

109. Realize an AND logic gate and OR logic gate using diodes

110. Explain the operation of NOT gate using a transistor

111. Write the symbol, truth table and output expression for I) OR ii) NAND iii) Ex-OR gate

112. Simplify the following Boolean expression and realize them using basic gates

Y = AC +AB + BC

113. Simplify the Boolean expression F = (A + E + C) (A+ B+C)(A+E) . Realize the simplified expression using only NAND gates

114. Write the truth table of an Ex-OR function and realize this using only NAND gates.
115.   Explain with an example the principle of duality in Boolean algebra.
116.   A logic circuit has three inputs and one output variable. The o/p is at logic 1 when two or more inputs are at logic 1. Write the truth table and realize this using NAND gates
117.   State and prove De Morgan's theorem for two variables
118.   Draw the logic circuit of the full adder and write its truth table.
119.   What is full adder? Draw the full adder block diagram using half adders and write its truth table
120.   With truth table, explain how RS flip flop can be realized using NOR gates.
121.   With truth table, explain how RS flip-flop can be realized using NAND gates.
122. Write the characteristic equations for Jk and D Flip Flops.
123. If the input frequency of TFF is 1600 kHz, what will be the output frequency?
124. How can a D flip flop be converted into T flip-flop?
125. What is meant by the term edge triggered?
126. Give the state diagram of Jk ff?
127. Draw the logic diagram of Master Slave Jk ff?
128. Write the characteristic equation of Jk ff and show Jk ff can be converted into T ff.
129. How many ff's are required to design a mod-7 up down counter?
130. Difference between Moore & mealy type sequential circuits
131. Distinguish between combinational & sequential logic circuits
132. What are the assumptions made for pulse mode circuit.
133. Distinguish between synchronous and asynchronous sequential circuits
134. What is an essential hazard and how to eliminate it?
135. What is race around condition?
136. What are the different modes of operation in asynchronous sequential circuits?
137. Define static 0 and static 1 hazard?
138. Distinguish between pulse mode and fundamental mode asynchronous sequential circuits.
139. What is meant by state assignment?
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145. Define static 0 and static 1 hazard?)
146. Distinguish between pulse mode and fundamental mode asynchronous sequential circuits.
147. What is meant by state assignment?
148. What are the different types of flip-flop?
149. What is the operation of RS flip-flop?
    • When R input is low and S input is high the Q output of flip-flop is set.
    • When R input is high and S input is low the Q output of flip-flop is reset.
    • When both the inputs R and S are low the output does not change

• When both the inputs R and S are high the output is unpredictable.

150. What is the operation of SR flip-flop?

   • When R input is low and S input is high the Q output of flip-flop is set.

   • When R input is high and S input is low the Q output of flip-flop is reset.

   • When both the inputs R and S are low the output does not change.

   • When both the inputs R and S are high the output is unpredictable.

151. What is the operation of D flip-flop? In D flip-flop during the occurrence of clock pulse if
D=1, the output Q is set and if D=0, the output is reset.

152. What is the operation of JK flip-flop?

   • When K input is low and J input is high the Q output of flip-flop is set.

   • When K input is high and J input is low the Q output of flip-flop is reset.

   • When both the inputs K and J are low the output does not change

   • When both the inputs K and J are high it is possible to set or reset the flip-flop (ie)
    the output toggle on the next positive clock edge.

153. What is the operation of T flip-flop? T flip-flop is also known as Toggle flip-flop.

   • When T=0 there is no change in the output.

   • When T=1 the output switch to the complement state (ie) the output toggles.

154. Define race around condition. In JK flip-flop output is fed back to the input. Therefore
change in the output results change in the input. Due to this in the positive half of the
clock pulse if both J and K are heighten output toggles continuously. This condition is
called 'race around condition'.

155. What is edge-triggered flip-flop? The problem of race around condition can solved by
edge triggering flip flop. The term edge triggering means that the flip-flop changes
state either at the positive edge or negative edge of the clock pulse and it is sensitive
to its inputs only at this transition of the clock.

156. What is a master-slave flip-flop?

157. Design a 3 bit up –down counter using Jk ff and explain its function with timing diagrams.

158. A sequential circuit has 2D ff's A and B an input x and output y is specified
by the following next state and output equations.

A (t+1)= Ax + Bx

B (t+1)= A'x

Y= (A+B) x'

   (i) Draw the logic diagram of the circuit.

   (ii) Derive the state table.

   (iii) Derive the state diagram.

159. Design a mod-6 counter FF'S. Draw the state transition diagram of the same.

160. a) Draw the clocked RS FF and explain with truth table.

   b) Write the excitation tables of SR, JK , D, and T Flip flops

161. a) Summarize the design procedure for synchronous sequential circuit.

   b) Realize D and T flip flops using Jk flip flops

162. Design a mod-10 synchronous counter using Jk ff. write excitation table and state Table.

163. Discuss the working of synchronous counter?
164. Discuss the design and working of an edge triggered flip-flop with preset and clear inputs ?
165. Discuss the working of a JK Master Slave flip-flop?
166. Discuss the working of decade counter (synchronous)?
167. Discuss construction and working of HEX counter (Mod-6 Ripple counter)?
168. What are ripple counters? Discuss its working?
169. What is a JK Flip Flop? Discuss the race around condition in that flip flop. How is it Rectified?
170. Draw the circuit diagram and explain the working of a decade ripple counter?
171. What are the advantages of synchronous counter?
172. Draw the logic diagram of Master Slave D Flip-Flop using NAND gates?
173. Draw the logic diagram of clocked RS Flip-Flop four NAND gates and explain its truth table?
174. Explain BCD counters with example?
175. What are shift register? Explain serial transfer of information using shift registers?
175. What is universal shift register? Draw the circuit of a 4-bit universal shift register.
176. Design 4-bit Ripple counter with D Flip-flops.
177. Discuss drawback of RS flip flop and how will these be removed?
178. Discuss a counter that has repeated sequence of six state. Draw the Excitation table and logic
       diagram of counter.
179. Discuss controlled shift registers. (PISO and Bidirectional shift register).
180. Differentiate Combinational and Sequential circuits?
181. What is the use of clear and preset inputs?
182. What do you mean by edge-triggering of Flip-Flop?
183. Differentiate Positive and negative edge triggering of the clock pulse?
184. Realize T-flip flop using JK flip-flop?
185. Explain sequential circuit with an neat sketch?
186. Define a Flip-Flop with a suitable sketch?
187. Draw the Basic flip-flop circuit.
188. Give the excitation table for JK flip-flop?
189. Explain the race around condition?
190. What is the state diagram?
191. Distinguish between combinational & sequential logic?
192. Give the characteristic table for JK flip-flop
193. Realize D Flip-flop using JK flip flop.
194. Realize the JK flip-flop using NAND gate only?
195. What is the excitation table for D flip-flop?
196. What are the advantages & disadvantages of synchronous over asynchronous counter?
197. Define edge triggering with a suitable example?
198. What is meant by a counter?
199. What is meant Universal shift register?
200. Mention the application of shift register.
201. Write the characteristic equation for a) JK Flip-flop b) T flip-flop c) D flip-flop

202. write the excitation table for a) T flip-flop b) SR flip-flop
203. Distinguish between Mealy and Moore's state machine with an example?
204. Design a counter with following repeated binary sequence 0,4,2,8, 1,6, 9 ….. using
    a) JK flip-flop
    b) D flip flop.
205. With relevant diagrams and truth table explain the operation 4 bit ripple counter.
206. Design a decade counter.
207 Design a counter using T flip-flop to count sequence 0,1,2,3,4,0,1,2…..
208 Design a 4-bit binary synchronous counter with a D Flip-flop
209 Design a 8-bit ring-counter with a suitable flip-flop.
210. Design a 4-bit switch-tail ring counter / Johnson counter with a suitable flip-flop.
211. Design a 4-bit Universal Shift Register
212. Design a following input sequence 01010110100 using the suitable logic.
213. Design a 4-bit Binary Up-Down Counter
214. Design a 4-bit BCD ripple counter with relevant diagram.
215. Draw the logic diagram of a 4-bit register with 4 D-Flip flops and four 4 x1 MUX's with
    mode selection inputs s0, s1. The register operation according to following func.
216. Design a 3 bit up –down counter using Jk ff and explain its function with timing diagrams.
217. A sequential circuit has 2D ff's A and B an input x and output y is specified by the
    following next state and output equations.
    A (t+1)= Ax + Bx
    B (t+1)= A'x
    Y= (A+B) x'
     (i) Draw the logic diagram of the circuit.   (ii) Derive the state table.
     (iii) Derive the state diagram.
218. Design a mod-6 counter FF'S. Draw the state transition diagram of the same.
    a) Draw the clocked RS FF and explain with truth table.
    b) Write the excitation tables of SR, JK , D, and T Flip flops
    c) Summarize the design procedure for synchronous sequential circuit.
    d) Realize D and T flip flops using Jk flip flops
219. Design a mod-10 synchronous counter using Jk ff. write excitation table and state table.
220. a. Give the comparison between
        1. Combinational circuits & Sequential circuits
        2. Synchronous sequential circuits & Asynchronous Sequential circuits
    b. Convert
        1. SR-flip-flop into JK flip –flop
        2. JK – flip-flop into T flip-flop
221. a. Draw & explain the block diagram of Moore & Mealy model?
    b. Explain the operation of
        1. 4 bit Serial –in- serial-out Shift Register
        2. 4-bit Serial-in-parallel – out Shift register