MCA-T112: Computer Organization & Architecture

Ob**jective Questions**

Unit-1

1. An 8-bit binary word b7b6b5b4b3b2b1b0 as an integer x ranges from
A) –128 to 128
B) –128 to 127
C) –256 to 256
D) None of the above

2. In a J-K flip-flop the function K = J is used to realize
A) T-Flip-flop
B) S-R Flip-flop
C) D-Flip-flop
D) M/S J-K flip-flop

3. A register capable of shifting its binary information in one or both direction is known as
A) Shift Register
B) Address Register
C) Index Register
D) Accumulator

4. . A micro programmemd control unit has a storage area called
A) memory
B) control memory
C) instruction memory
D) noen

5. What logic circuit would you use for addressing memory?
A) Full adder
B) Multiplexer
C) Decoder
D) Direct Memory Access circuit

6. How many select lines do an 8 input multiplexer have?
A) 1
B) 3
C) 8
D) 64

7. How is a *J-K* flip-flop made to toggle?

A) J=0, K=0

B) J=1, K=0

C) J=0, K=1

D) J=1, K=1

8. 8085 Microprocessor Uses --------V Power supply
A**) 5**
B) 10
C) 8
D) 6

9. On a master-slave flip-flop, when is the master enabled?
When the gate is Low
When the gate is HIGH
Both of the above
Neither of the above

10. How many flip-flops are required to make a MOD-32 binary counter?
A) 3
B) 45
C) 5
D) 6

11. A MOD-16 ripple counter is holding the count 1001_2. What will the count be after 31 clock pulses?
A) 1000_2
B) 1010_2
C) 1011_2
D) 1101_2

12. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
A) 0000
B) 0010
C) 1000
D) 1111

13. What is a shift register that will accept a parallel input, or a bidirectional serial load and internal shift features, called?
A) Tristate
B) End around
C) Universal
D) Conversion

14. A bidirectional 4-bit shift register is storing the nibble 1101. Its $\text{RIGHT}/\overline{\text{LEFT}}$ input is

HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____.

A) 1101
B) 0111
C) 0001
D) 1110

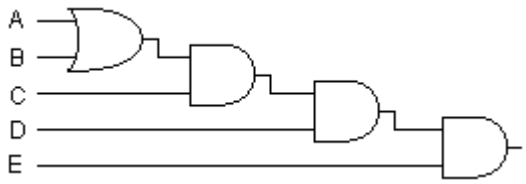
15. Determine the values of A, B, C, and D that make the sum term $\overline{A}+B+\overline{C}+D$ equal to zero.

A = 1, B = 0, C = 0, D = 0
A = 1, B = 0, C = 1, D = 0
A = 0, B = 1, C = 0, D = 0
A = 1, B = 0, C = 1, D = 1

16. Which of the following expressions is in the sum-of-products (SOP) form?

A) $(A + B)(C + D)$
B) $(A)B(CD)$
C) $AB(CD)$
D) $AB + CD$

Derive the Boolean expression for the logic circuit shown below:



A) C(A+B)DE’

B) [C(A+B)D+E’]

C) [[C(A+B])D]E’

D) ABCDE

18. When used with an IC, what does the term "QUAD" indicate?

A) 2 Circuits
B) 4 Circuits
C) 6 Circuits
D) 8 Circuits

19. A flip flop circuit can be used for

A) Counting
B) Scaling
C) Rectification
D) Demodulation

20. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will

result in a HIGH output?
A) 1
B) 2
C) 7
D) 8

Unit-2

1. Which 0 is inserted to the end bit position
A) logical shift
B) arithmetic shift
C) cyclic shift

2. Microprograms ar designed to _____ the behaviour of the instruction set.
A) emulte
B) input
C) register
D) hardwired

3. The communication line between the CPU, memory and peripherals is called a
A)Bus B) line C)media D) none of these

4. Status register is also called as _____
A) Accumulator B) Stack C) Counter D) flags

5 Which of the following addressing mode is used in zero-address instructions.
A)direct
B)implied
C)indirect
D)none

6. Where does a computer add and compare data?
A) Hard disk
B) Floppy disk
C) CPU chip
D) Memory chip

7.. A micro programmemd control unit has a storage area called
A) memory
B) control memory
C) instruction memory
D) noen

8. A complete microcomputer system consists of
A) microprocessor
B) memory
C) peripheral equipment
D) all of above

9. Number of addressing modes used in CISC architectures are
A) 1 to 5
B) 5 to 10
C) 5 to 20
D) above 20

10. Pipelining strategy is called implement
A) instruction execution
B) instruction prefetch
C) instruction decoding
D) instruction manipulation

11. A stack is
A) an 8-bit register in the microprocessor
B) a 16-bit register in the microprocessor
C) a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer
D) a 16-bit memory address stored in the program counter

12. A stack pointer is
A) a 16-bit register in the microprocessor that indicate the beginning of the stack memory.
B) a register that decodes and executes 16-bit arithmetic expression.
C) The first memory location where a subroutine address is storeD)
D) a register in which flag bits are stored

13.The branch logic that provides decision making capabilities in the control unit is known as
A) controlled transfer
B) conditional transfer
C) unconditional transfer
D) none of above\

14. Interrupts which are initiated by an instruction are
A) internal
B) external
C) hardware
D) software

15. A skip instruction is a _____address instruction.
A) zero
B) one
C) two
D) three

16. The reason why micro-programmed control unit is advantages are
A) easy to change of micro-programs

B) slow speed
C) operating system and high-level language support
D) costly

17. Instruction register is a
A) General purpose register
B) Uservisible register
C) Control and status register
D) None

18. long distance communication which of the following are suitable.
A) Synchronous serial data transrer
B) Asynchronous serial data transfer
C) Synchronous parallel data transfer.
D) Asynchronous parallel data transfer.

19. purpose of data link protocol is/are
A) Establish and terminate a connection two communicating units.
B) Identify the sender and receiver.
C) Handling transmission errors.
D) None.

20. The number of bits required for the operation code of an instruction depends on the
A) number of operations available
B) number of operands
C) both a and b
D) none

Unit-3

1. A CPU handles interrupt by executing interrupt service routine
A) Whenever an interrupt is registereD)
B) By checking interrupt register after execution of each instruction
C) By checking interrupt register at the end of fetch cycle.
D) By checking interrupt register at regular times interval.

2. The CPU state is saved in the event of a transfer control.
A) From one instruction to a non-sequential instruction of a program.
B) From one program to another.
C) During execution of an instruction due to an interrupt cycle.
D) None

3. I/O interfaces are used because
A) Data format and codes in peripherals are differ from that are used in CPU and memory.
B) Data transfer rate is slwer than that of the CPU.
C) Addressing I/O devices are difficult task for CPU.

D) All of these

4. Whch of the following statements are for I/O buses:
A) The I/O bus consists of address, control and data lines.
B) I/O devices and I/O interfaces are attached via I/O bus.
C) The I/O bus from the processor is attached to all peripheral interfaces.
D) There is no concept of I/O bus.

5. In shich of the following accessing method of I/O devices, the computer has an independent set of data, control and address buses, one for accessing memory and another for accessing I/O.
A) Isoloated I/O method
B) Memory mapped method
C) Input-Output Processor
D) DMA

6. The strobe method of asynchronous data transfer is not useful because
A) When source unit actives the strobe, there is no way of knowing whether the destination unit has received data A)
B) When destination unit actives the strobe, there is n way of knowing whther the Source unit has received data A)
C) Strobe control is not properly used by the other side of communicating device.
D) Processor is not able to respond the strobe contrl efficiently.

7. Which of the following statement(s) are correct for asynchronous serial transfer.
A) Data is sent only when the communication line is idle.
B) Only when other sides of communicating object is ready.
C) Both statements are true.
D) None.

8. The interrupt-initiated I/O method is used for
A)Transferring data to and from peripherals.
B) Transferring data to and from memory.
C) Transferring data to processor only.
D) All

9. An I/O processor is capable for
A) Having complete control over I/O operation.
B) Executing I/O instructions.
C) Instructing by the CPU to initiates the I/O transfer.
D) All

10. Whe the CPU wants to read a block data, it issues a command to the DMA by sending some information, which othe the following information(s) is/are not send by it
A) Control signal which specifies the read operation.
B) Address of the specific I/O device.
C) Next instruction address to be executeD)

D) Staarting address in memory to read from

11. Which type of interrupts can be enabled/disabled by program instruction.
A) Maskable
B) Non maskable
C) Vectored
D) Software interrupts.

12. An example of an exception is
A) Sending I/O request by the processor.
B) Executint the user program in supervisor mode.
C) Transfer the program control to other location non-sequentially.
D) Saving the information of currently executing instruction on to the stack.

13. For long distance communication which of the following are suitable.
E) Synchronous serial data transrer
F) Asynchronous serial data transfer
G) Synchronous parallel data transfer.
H) Asynchronous parallel data transfer.

14. The purpose of data link protocol is/are
E) Establish and terminate a connection two communicating units.
F) Identify the sender and receiver.
G) Handling transmission errors.
H) None.

15. The frame check field in the bit-oriented protocol is of_____bit.
A) 8
B) 16
C) 32
D) 64

16. The priority scheme _____is implemented by software means.
A) Polling
B) Handshaking
C) Strobe
D) None

17. A _____device is used to convert ditital to anolog conversion and vice-versa in serial communication.
A) Memory
B) Modem
C) I/O interface
D) All

18. The _____I/O method uses the same address space for both memory and I/O.
A) Non isolated
B) Bidirectional

C) Isolated
D) None.

19. Using programmed I/O, the system throughput _____as number of I/O device connected in the system increases.
A) Decreases
B) Retain
C) Consistance
D) Increases

20. In case of using IOP, _____ is act as message centre where each processor leaves information for the other.
A) Polling
B) Modem
C) All
D) Memory

Unit-4

1. Which of the following property allows the processor to execute a number of clustered locations.
A) Spatial
B) Temporal
C) Inclusion
D) Coherence

2. Which of the following factors do not affects the hit ration of cache
A) Block replacement algorithms.
B) Blcok frame size
C) Cycle counts
D) Main memory size

3. Which of the followint replacement policies, yield the ;better hit ratio:
A) FIFO
B) LRU
C) LFU
D) OPT

4. The main goal of replacemtn algorithm is
A) To make room for another page
B) To degrade the page miss-ratio
C) To minimize the number of page faults
D) Only just replace the page

5. In a given virtual address, high order bits specifies
A) Page number
B) Line number

C) Word in particular page
D) None

6. The logical address is mapped ito physical address requires____table
A) 1
B) 2
C) 3
D) None

7. In which of the mapping function, there is no need of replacement algorithm
A) Direct
B) Set-associative mapping
C) Full associative mapping
D) All

8. On which of the following factors, hit ratio does not depend
A) Line size
B) Set size
C) Cache size
D) None

9. The cache speed is affect by underlying SRAM/DRAM technology Implemented cache organization
A) Cache hit ratio
B) All
C) Miss
D) None

10. In a direct mapping, the index field equals to sum of
A) Tag and word fields
B) Block and word fields
C) Tag an block fields
D) Any of b or c

11. A mapping function which dos not restricts any block to be copied any where in the cache is
A) Direct
B) Full associative mapping
C) Set associative mapping
D) Not possible

12 If m=2r be the nuber of block frames in cache. Let b=2w be the size of each block and bock frames. So total words that can be stored in cache memory is given by
A) 2^{r+w}
B) 2^{r-w}
C) r+w
D) r-w

13. Which of the following applications are not implemented with ROMs:
A) Bootstrap loader
B) Startup program
C) Tables of constants
D) Translator

14. Flash memory is the example of
A) Read-write memory
B) Read-Only memory
C) Read –mostly memory
D) Optical memory.

15. The time taken for beginning of the sector to reach the head is known as
A) Seek time
B) Rotational delay
C) Access time
D) Data transfer time

16. Which part of compute syster supervises the flow of information between auxillary and main memory
A) Memory management system
B) Virtual memory system
C) Cache memory
D) None

17. Which of the following parameters are not related with magnetic disks.
A) transfer time
B) Rotational latency
C) Addressing capability
D) Access time

18. In the hardware organizatiuon of associative memory, which of the following register are used to provide mask bits for a particular fielD)
A) Argument register
B) Key register
C) Match register.
D) None

19. The field which uniquely identifies the requested data in a given block is
A) Tag
B) Block
C) Word/offset
D) None

20. In _____memory, data are accessed by its content rather than its location.
A) Cache
B) Read only memory
C) Random access memory

D) Associative

Unit-5

1. The software used to drive microprocessor-based systems is called:
A**) Assembly Language**
B) Firmwate
C) Machine Language Code
D) Basic Interpreter Instruction

2. The _____ ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus
A) control bus
B) Control Instructins
C) Address decoder
D) CPU

3. Single-bit indicators that may be set or cleared to show the results of logical or arithmetic operations are the:
A) Flags
B) Registers
C) Monitors
D) Decisions

4. When referring to instruction words, a mnemonic is:
A) a short abbreviation for the operand address
B) a short abbreviation for the operation to be performed
C) a short abbreviation for the data word stored at the operand address
D) shorthand for machine language

5. The 8085A is a(n):
A) 16- bit parallel CPU
B) 8-bit serial CPU
C) 8-bit parallel CPU
D) None

5. A register in the microprocessor that keeps track of the answer or results of any arithmetic or logic operation is the:
A) stack pointer
B) program counter
C) instruction pointer
D) accumulator

6. What is the difference between a mnemonic code and machine code?
A) There is no difference.
B) Machine codes are in binary, mnemonic codes are in shorthand English.
C) Machine codes are in shorthand English, mnemonic codes are in binary

7. Which bus is a bidirectional bus?
A) Address bus
B) Data bus
C) Address bus and data bus
D) None of the above

8. What kind of computer program is used to convert mnemonic code to machine code?
A) Debug
B) Assembler
C) C++
D) Forton

.10. Pipelining strategy is called implement
A) instruction execution
B) instruction prefetch
C) instruction decoding
D) instruction manipulation

11. The MFC signal is generated by the
A) addressed device
B) processor
C) none
D) memory

12. Which of the following is not a basic element within the microprocessor?
A) Microcontroller
B) Arithmetic logic unit
C) Register array
D) Control unit

12. Which of the following is not an enhancement to the Pentium that was unavailable in the 8086/8088?
A) "Pipelined" architecture
B) Expansion of cache memory
C) Inclusion of an internal math coprocessor
D) Data/address line multiplexing

13. The first microprocessor had a(n)_____.
A) 1-bit data bus
B) 2- bit data bus
C) 4- bit data bus
D) 8- bit data bus

14. Which microprocessor has multiplexed data and address lines?
A) 8086/8088
B) 80286
C) 80386
D) Pentium

15. Which of the following is not a jump instruction?
JB (jump back)
JA (jump above)
JO (jump if overflow)
JMP (unconditional jump)

16. Which of the following was not a design improvement for the 8086/8088 over the 8085?
A) Execution unit (EU)
B) 16-bit data bus
C) Arithmetic logic unit (ALU)
D) Bus interface unit (BIU)

17. Which of the following is not an arithmetic instruction?
A) INC (increment)
B) CMP (compare)
C) DEC (decrement)
D) ROL (rotate left)

18. The first Intel microprocessor to contain on-board cache memory was the _____.
A) 80386
B) 80486
C) Pentium
D) Pentium Pro

19. Which of the following is not an 8086/8088 general-purpose register?
A) Code segment
B) Data segment
C) Stack segment
D) Address segment

20. The Pentium can address _____.
A) 1 MB
B) 1 GB
C) 2 GB
D) 4 GB

Short Answer Type Questions

Unit-1

1. Design a four bit combinational circuit decrementer using full adder circuits.
2. Derive a combinational circuit that selects and generates any of the 16 logic functions.
3. An 8 bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.
4. What is the shortcoming of an S-R flip flop? Explain how this shortcoming is removed in J-K flip flops.
5. What is a mod-5 counter? How is it built? How is a decade counter realized using mod-5 counter?
6. What do you understand by fan-in and fan-out of a logic gate?
7. What is triggerinbg of flip-flops? Discuss different types of triggering with examples?
8. Explain the term 'UP Counter', "DOWN Counter", and UP/DOWN Counter.
9. Discuss Underflow and Overflow phenomenon which occur in digital computer.
10. Simplify the function Y=ABC'+ABC by Karnaugh Map.

Unit-2

1. Let SP=000000 in the stack. How many items are there in the stack if:
    a. FULL=1 and EMTY=0?
    b. FULL=0 and EMTY=1?
2. convert the following expression from infix to reverse Polish notation.
   A*B + C*D +E*F
3. Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result.
   (3+4)[10(2+6)+8]
4. Define auto increment & auto decrement mode of addressing?
5. Which data structure is best supported using indirect addressing mode?
6. What do you known by control worlD)
7. Differentiate b/w RISC and CISC?
8. What are the types of microinstructions available?
9. Explain the multiple bus organization in detail
10. Write an program to evaluate (A+B)*(C+D) using one address instructions.
11. What is the need of addressing mode.
12. explain status bit condition in program control.

Unit-3

1. Draw a neat diagram of connection of I/O bus to input-Output devices.
2. differentiate b/w strobe vs handshaking process.
3. write a diagram for destination initiated strobe for data transfer.
4. Explain Start bit and stop bit in Asynchronous data transfer.
5. What is modes of transfer, How many types of it.

6. What is the importance of I/O interface? Compare the features of SCSI and PCI interfaces.
7. Discuss the DMA driven data transfer technique.
8. Explain in detail about standard I/O interface.
9. What is port? What are the types of port available?
10. What is PCI bus?
11. What are the different methods used for handling the situation when multiple interrupts occurs?
12. Write the factors considered in designing an I/O subsystem?

Unit-4

1. Define Memory Access time for a computer system with two levels of caches
2. List the factors that determine the storage device performance.
3. List the various semiconductors RAMs?
4. What will be the width of address and data buses for a 512K * 8 memory chip?
5. What is the mapping procedures adopted in the organization of a cache Memory?
6. Define Hit and Miss rate?
7. What is meant by memory interleaving?
8. What is meant by memory management unit?
9. What are the enhancements used in the memory management?
10. Give the structure of semiconductor RAM memories. Explain the read and write operations in detail?
11. Explain the concept of memory hierarchy?
12. A digital computer has a memory unit of 64K*16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the caches accommodate?

Unit-5

1. Where does CPU Enhanced mode originate from?
2. How many different instructions mP 8085 has? What is an instruction set?.
3. How the mnemonics written in assembly language are translated into binary?
4. What are the jobs that a microcomputer is capable of doing? How does it do the jobs?
5. What are the different buses and what jobs they do in a microprocessor?
6. Draw the software hierarchy of a microcomputer system
7. What is a coprocessor?
8. Draw a typical coprocessor configuration and discuss the same.
9. In how many groups can the signals of 8085 be classified?
10. The address capability of 8085 is 64 KB. Explain

Long Answer Type Questions

Unit-1

1. What are presettable counters? What is the nature of modulus of a presettable counter?
2. What are demultiplexers/decoders? What is the difference between a demultiplexer/decoder? Show connection diagram of a demultiplexer and decoder.
3. Draw the schematic diagram of a master-slave J-K flip-flop? Discuss its working principle. What are its advantages over other types of flip-flops.
4. What is D flip-flop? What is its advantage over S-R flip-flop? What is the difference between a D latch and a D flip-flop?
5. How is an n-bit adder realized using n full- adders? Draw the logic network.
6. Find the simplified Boolean function
    a. in sum of products form
    b. in product of sums form for the Karnaugh map represented by
    Y(A,B,C,D)=m(0,3,7,8,9,11,12,13)+ Zd(1,4,14,15)

Unit-2

1. A two word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is
    A) Direct B) Indirect c Relative D) IndexeD)
2. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the in instruction is in one memory word)
3. Give five examples of external interrupts and five examples of internal interrupts. What is the difference between a software interrupt and a subroutine call?
4. Explain the working of register set with common ALU with neat diagram.
5. Given the 16 bit value 1001101011001101. What operation must be performed in order to:
    A) Clear to 0 the first eight bits?
    B) set to 1 the last eight bits?
    C) complement the middle eight bits?
6. A stack is organized such that SP always points at the next empty location on the stack. This means that SP can be initialized to 4000. and the first item in the stack is stored in location 4000. List the microoperations for the push and pop operations.

Unit-3

1. A DMA controller transfers 16 bits words to memory using cycle stealing. The words are assembled fromk a device that transmits characters at a rate of 2400 characters per seconD) The CPU is fetching and executing instructions at an average rate of 1 million instructions per seconD) By how much will the CPU be slowed down because of DMA transfer?
2. How many characters per second ca be transmitted over a 1200 baud line in each of the following modes? (Assume a character codoe of eight bits.)
    a. Synchronous serial transmission.
    b. Asynchronous serial transmission with two strop bits.
    c. Asynchronous serial transmission with one stop bit.
3. What is the importance of I/O interface? Compare the features of SCSI and PCI interfaces.
4. Explain the use of vectored interrupts in processes. Why is priority handling desired interrupt controllers? How does the different priority scheme work?
5. What do you understand by the terms I/O interface, I/O processor and interrupt mask? Explain with the help of diagrams.
6. Explain the working of a DMA controller.

Unit-4

1. A computer system has a main memory consisting of 16 M words. It also has a 32Kword cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.
   • Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format.
   • How will the main memory address look like for a fully associative mapped cache?
2. Give the basic cell of an associative memory and explain its operation. Show how associative memories can be constructed using this basic cell.
3. Give the format for main memory address using associative mapping function for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.
4. How to construct an 8M * 32 memory using 512 K * 8 memory chips.
5. Explain Set associative mapping procedure with set size 4 .
6. Explain the concept of virtual memory with any one virtual memory management technique.

Unit-5

1. Discuss the two registers program counter and stack pointer, and also discuss the function of ALE and how does it function?
2. Mention the following:
   (*a*) Control and Status signals
   (*b*) Interrupt signals
   (*c*) Serial I/O signals
   (*d*) DMA signals
   (*e*) Reset signals.
3. Draw the lower and higher order address bus during the machine cycles.
4. What is meant by Bus Idle Machine cycle? and also Discuss the concept of WAIT states in microprocessors.
5. Draw the diagram which will show the three buses separately, with the help of peripheral ICs.
6. Explain the difference between HLT and HOLD states. And Indicate the length of the Program Counter (PC) to access 1 KB and 1 MB memory.