AALIM MUHAMMED SALEGH COLLEGE OF ENGINEERING,AVADI(IAF),CHENNAI-55

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MODEL EXAMINATION

QUESTION PAPER I

SUB/CODE: VLSI DESIGN/EC2354 **MAXIMUM MARKS:100**

YEAR/SEM/SEC: III/VI/A,B,C

PART-A(2*10= 20)

1. Why is NMOS technology more preferred than PMOS technology?
2. What is body effect ?
3. Define Elmore delay with necessary equations.
4. What is gate shrink ? How does it affect power and delay?
5. Draw an AOI21 gate. Estimate its logical effort and parasitic delay.
6. Define clock skew.Also, enumerate on the factors that cause timing failures.
7. What is silicon debug?
8. Define fault coverage and controllability.
9. What is inertial delay?
10. What are reduction operators?

PART-B(16 * 5 = 80)

11. (a)Explain the DC transfer characteristics of CMOS inverter (10)
    (b) An n-MOS transistor has a nominal threshold voltage of 0.16 V. Determine the shift in the threshold voltage caused by body effect using the following data. The n-MOS is operating at a temperature of 300°K with the following parameters. Gate oxide thickness(t_{ox})= 0.2 x10^{-5} cm, relative permittivity of oxide(ε_{ox}) = 3.9,relative permittivity of silicon(ε_{si})= 11.7, substrate bias voltage =2.5 V, Intinsic electron concentration(N_i) = 1.5 x10^{10}/ cm^3, impurity concentration in substrate (N_A) = 3 x10^{16}/ cm^3. Given Boltzmann's constant = 1.38 x 10^{-23} J/°K, electron charge = 1.6 x 10^{-19} Coulomb and permittivity of free space = = 8.85 x 10^{-14} F/cm (6)

(or)

12. (a)Explain photolithography, gate/source/drain formation and isolation steps of CMOS fabrication process with neat diagrams. (8)
    (b) Draw the schematic and Physical design of 2 input CMOS NAND gate (8)
13. Explain logical effort and transistor sizing in multistage logic networks and derive the expressions for the best number of stages to minimize delay. (16)

(or)

14. (a)Explain the concept of static and dynamic power dissipation in CMOS circuits. (8)
    (b) Discuss the principle on Constant field scaling and its effect on device characteristics.(8)

15. (a)Explain in detail about Dynamic circuit families (10)
    (b) Implement a 2:1 Mux using various circuit families (6)

(or)

16. Explain in detail the sequencing methods needed to sequence static circuits (16)
17. Explain the Design for testability(DFT) concepts (16)

(or)

18. Explain (a) Silicon debug principles (6)
    (b)Scan Based Design techniques. (10)
19. (a) Write the dataflow modeling for a 4:1 MUX using Verilog HDL (8)
    (b) Explain the different timing controls available in Verilog HDL (8)

(or)

20. (a) Explain assignment statements in verilog with suitable examples (8)
    (b) Write a behavioral level description of a 2 bit comparator using Verilog HDL (8)

AALIM MUHAMMED SALEGH COLLEGE OF ENGINEERING,AVADI(IAF),CHENNAI-55

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MODEL EXAMINATION

QUESTION PAPER II

SUB/CODE: VLSI DESIGN/EC2354 **MAXIMUM MARKS:100**

YEAR/SEM/SEC: III/VI/A,B,C

PART-A(2*10= 20)

1. What are the different operating regions ofa MOS transistor?
2. What is channel length modulation?
3. Write the expressions for logical effort and parasitic delay of an n-input NOR gate.
4. What is TDDB ?
5. What are the merits and demerits of CVSL over static CMOS circuits.
6. Define sequencing overhead.
7. What is fault model?
8. Define ATPG.
9. Differentiate always and initial statements.
10. Write a verilog program for a 1 bit full adder.

PART-B(16 *5 = 80)

11. (a) An n-MOS transistor has the following parameters.Gate oxide thickness(t_{ox})=10 nm, relative permittivity of oxide(ε_{ox}) = 3.9, electron mobility= 520 cm^2/V-sec, threshold voltage =0.7 V, permittivity of free space = = 8.85 x 10^{-14} F/cm and (W/L)= 8. Calculate the drain current when (V_{gs} = 2 V and V_{ds} =1. 2 V **)** and (V_{gs} = 2 V and V_{ds} =2 V **) .** Also compute the gate oxide capacitance per unit area. W and L refer to the width and Length of the channel respectively. (6)
    (b) Explain the Secondary effects of MOS transistors in detail (10)

(or)

12. (a)Explain in detail the fabrication process of n-MOS transistor with neat diagrams. (10)
    (b) Discuss in detail with a neat layout, the design rules for a CMOS inverter. (6)
13. (a)Estimate the delay of an inverter driving 'h' identical inverters. Thereby, estimate the delay of FO4 inverter. Assume inverter is constructed in a 180 nm process with τ= 15 ps. (6)
    (b)Explain Reliability terminology and reliability related issues in detail (10)

(or)

14. (a)Explain Different Device MOS Models with the necessary equations (8)
    (b)How can Circuits be characterized using SPICE ? (8)

15. (a)Explain in detail about Static/Ratioless circuit family. (10)
    (b) Explain DCVS circuit family (6)

(or)

16. (a)Explain in detail about Clock skew and Time borrowing concepts that cut into the effective period available for computation. (8)
    (b)Write short notes on sequencing Dynamic circuits (8)
17. (a)With necessary circuit modules, explain BIST techniques. (10)
    (b)Write short notes on Testers,Test fixutures and Test programs (6)

(or)

18. Explain Manufacturing Test principles in detail (16)
19. Design and develop a HDL project for a 4 bit synchronous counter using structural modeling. Also, realize a test bench program to simulate the counter. (16)

(or)

20. (a) Explain conditional and looping statements in Verilog with suitable examples. (8)
    (b)Explain how gate delays can be modeled in Verilog. (8)

AALIM MUHAMMED SALEGH COLLEGE OF ENGINEERING,AVADI(IAF),CHENNAI-55

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MODEL EXAMINATION

QUESTION PAPER III

SUB/CODE: VLSI DESIGN/EC2354 **MAXIMUM MARKS:100**

YEAR/SEM/SEC: III/VI/A,B,C

PART-A(2*10= 20)

1. Define threshold voltage.
2. Define feature size and state the objectives of layout design rules.
3. Define crosstalk.
4. What is charge sharing?
5. Compare CMOS and Pseudo- n-MOS circuit families.
6. Define setup time and setup time failure.
7. List the basic types of CMOS testing.
8. What is Delay fault testing?
9. Define instance and instantiation with a suitable example.
10. Differentiate == and === verilog operators.

PART-B(16 *5 = 80)

11. (a)Derive the equations for Drain current of MOS transistor. Discuss the relevant regions for n-MOS transistor operations with relevant graphs. (8)
    (b)Write short notes on Velocity Saturation and Channel Length modulation (8)

(or)

12. (a)Explain CMOS process enhancement techniques in detail (10)
    (b) Discuss about design rule background. (6)
13. (a) Explain in delay about RC delay estimation with suitable examples. (10)
    (b) Write short notes on reducing Static and Dynamic power reduction (6)

(or)

14. (a)How do you perform DC analysis of a transistor using SPICE ? (6)
    (b) How are MOS device characteristics estimated using SPICE? (10)
15. (a) Realize transistor level schematic of the logic function Z=(A(D+E)+BC)' using Static CMOS and choose transistor sizes to achieve equal rise and fall time. (8)
    (b) Explain Asymmetric gates and Input ordering delay effect in static CMOS family (8)

(or)

16. Explain In detail about Synchronizers and concept of metastability (16)

17. Explain System level testing/Boundary Scan testing in detail (16)

(or)

18. Explain adhoc testing and scan based approaches for design for testability (16)
19. (a) Draw a 3:8 Decoder using NAND gates and realize a Gate level Verilog description for the same (8)
    (b) Explain the different ways of specifying delays in continuous assignment statements (8)

(or)

20. (a)Enumerate operators, operands and expressions in Verilog with suitable examples (10)
    (b)Explain blocking and non blocking assignments with suitable examples. (6)