**MSVD03**

**MTCSE16C3/MTETE16C3**

**MODEL QUE PAPERS**

**M.TECH**

**IV Semester**

**SPE: (VLSI DESIGN)**

**VERILOG HARDWARE DESCRIPTION LANGUAGE**

Time: 3 Hours Max. Marks: 75

 ***INSTRUCTIONS:***

* *Question paper is divided into three groups.*
* *Each group is of 25 marks.*
* *Figure to the right in bracket indicates mark.*
* *Assume suitable data if necessary.*

**GROUP A : Answer any three questions. (Question No. 1 is compulsory)**

Q.1 Explain ports with types. (05)

Q.2 What are the file input output functions? (10)

Q.3. What do you mean by operator? (10)

Q.4. Explain combinatorial UDP along with one example (10)

Q.5. Explain laxical conventions. (10)

**GROUP B : Answer any three questions. (Question No. 6 is compulsory)**

Q.6 Explain identifiers with example. (05)

Q.7 What is String and Multi dimensional array? (10)

Q 8. Explain parameterized modules along with one example. (10)

Q 9. Explain state machine types. (10)

Q.10. Enumerate and explain loop statement. (10)

**GROUP C: All Questions are Compulsory.**

**Q.11 Fill in the blanks (Each question carries 2 marks)**

(i) Modules can have \_\_\_\_\_\_\_\_\_\_.

(ii) \_\_\_\_\_\_\_\_\_\_\_\_ is the names you give your wires, gates, functions.

(iii) UDPS always have \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ input.

(iv) Z mems \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

(v) String are stored in \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

**Q.12 Multiple choice question. (Each question carries 2 marks)**

(i) Every system has a delay before it is \_\_\_\_\_\_\_\_.

 (a) Execution

 (b) Run

 (c) Compile

 (d) Design

(ii) Output ports can have \_\_\_\_\_\_\_\_\_\_.

 (a) Controls

 (b) Registers

 (c) Wires

 (d) Modules

(iii) For sequential VDP, f stands for \_\_\_\_\_\_\_\_\_\_.

1. Rising edge
2. Falling edge
3. Any change
4. None of these

(iv) Take contains \_\_\_\_\_\_\_\_\_ statement.

1. Single
2. Double
3. Triple
4. None of these

(v) Function must take \_\_\_\_\_\_\_\_\_\_ time.

(a) One

 (b) Two

 (c) Zero

 (d) Four

**Q.13 True or false (Each question carries 1 marks)**

(i) Every wire and reg in verilog starts out unknown.

(ii) Parameters are run time constants.

(iii) Function must return the value.

(iv) Concentration can be used on one sides of an assignment.

(v) The wait statement if it is condition is true.

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