**MSVD02**

**MTCSE16C2/MTETE16C2**

**MODEL QUE PAPERS**

**M.TECH**

**IV Semester**

**SPE: (VLSI DESIGN)**

**DIGITAL VLSI DESIGN**

Time: 3 Hours Max. Marks: 75

***INSTRUCTIONS:***

* *Question paper is divided into three groups.*
* *Each group is of 25 marks.*
* *Figure to the right in bracket indicates mark.*
* *Assume suitable data if necessary.*

**GROUP A : Answer any three questions. (Question No. 1 is compulsory)**

Q.1 Explain the CMOS lambda based design rules (05)

Q.2 Explain the BICMOS Inverter. (10)

Q.3. Draw and explain small signal model of MOS. (10)

Q.4. Explain two stage MOS operational amplifier design criteria    (10)

Q.5. How analysis of differential amplifier can be done by using active load. (10)

**GROUP B : Answer any three questions. (Question No. 6 is compulsory)**

Q.6 Explain direct coupled FET logic inverter. (05)

Q.7 Explain carry slip adder. Give optimization of carry slip adder (10)

Q.8 Explain resistances and capacitances estimation. (10)

Q.9 What is n by m RAM using parameterized modules? Explain. (10)

Q.10 Design arithmetic logic unit. (10)

**GROUP C: All Questions are Compulsory.**

**Q.11 Fill in the blanks (Each question carries 2 marks)**

(i) Switch logic is based on\_\_\_\_\_\_\_ or trasmission gates.

(ii) As the separation between metal-semiconductor surface is reduced,the charge stored in the device \_\_\_\_\_.

(iii) Capture mode is used for  \_\_\_\_\_\_\_\_\_\_\_.

(iv) VCO is used for \_\_\_\_\_\_\_\_in communication field.

(v) Resolution of  8 bit A to D converter is \_\_\_\_\_\_\_\_.

**Q.12 Multiple choice question. (Each question carries 2 marks)**

(i) Which of the following processing techniques would be used to create the source and drain regions of a transistor?

(a) Oxidation

(b) Ion implantation

(c) Sputtering

(d) Polysilicon deposition

(ii) The capacitance of a transistor gate is proportional to what?

(a) The width of the gate

(b) The length of the gate

(c) The area of the gate

(d) The depth of the channel

(iii) Which addition is correct

(a) 0101+1111=11010

(b) 0101+1111=10100

(c) 0101+1111=11001

(iv) In N channel MOSFET with gate reverse biased, the gate current is of the order of

(a) 10­-3amp

(b) 10-6amp

(c) 10-9 amp

(d) 10-12amp

(v) Given BCD 10010011,its decimal equivalent is

(a) 147

(b) 143

(c) 93

(d) 39

**Q.13 True or false (Each question carries 1 marks)**

(i) The area capacitances are associated with layers to substrate & from gate to channel.

(ii) The ion implementation is achieved by bombarding high velocity electron on semiconductor surface.

(iii) CMOS logic family takes minimum power.

(iv) NOT gate cannot implemented by transistor.

(v) The meaning of decoder is many to one.

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