Department of Computer Science & Engineering

QUESTION BANK

Subject: DLD   **Faculty: P.Siva Ram Prasad**
Branch: II CSE I Sem

UNIT - I

1. Convert the following number with indicated bases to decimal [4×2=8]
   i) $(1\ 0\ 1\ 1\ 1\ 1)2 =$ ii. $(A\ 3\ B)16 =$ iii. $(2\ 3\ 7)8 =$ iv. $(4\ 3)5 =$
2. Obtain the 1's and 2's complements of the following binary numbers [4×2=8]
   i. $1\ 1\ 1\ 0\ 1\ 0\ 1\ 0 =$ ii. $0\ 1\ 1\ 1\ 1\ 1\ 1\ 0 =$ iii. $1\ 0\ 0\ 0\ 0\ 0\ 0\ 0 =$ iv. $0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 =$
3. Convert the following numbers. [4×=8] i. $(53)10 = (\ )2$ ii. $(231)4 = (\ )10$ iii. $(1\ 1\ 0\ 1\ 1\ 0\ 1)2 = (\ )8$
   iv. $(4D.56)16 = (\ )2$
4. Add and subtract in binary [4×=8]   i. $1\ 1\ 1\ 1$ and $1\ 0\ 1\ 0$ ii. $1\ 1\ 0\ 1\ 1\ 0$ and $1\ 1\ 1\ 0\ 1$ iii. $1\ 0\ 0\ 1\ 0\ 0$ and $1\ 0\ 1\ 1\ 0$ iv. $1\ 1\ 0\ 1\ 0\ 0\ 1$ and $1\ 1\ 0\ 1\ 1$
5. Perform the following binary multiplication operations i. $100010 \times 001010 =$ ii. $001100 \times 011001 =$ iii. $000100 \times 010101 =$
6. Write the one's and two's complements of the following example. i. 0011001 ii. 1110011 iii. 111111
7. Find the decimal equivalent of the following two's complement numbers. i. 11111 ii. 10001
   iii. 01010 iv. 10011 v. 10101
8. Explain about error Detecting code with example.

UNIT - II

1. Simplify each of the following expressions   i. $ABCD + ABCD + CD$ ii. $(A + B)(A + B + D)(B + C + D)$
2. Explain about positive and Negative logic in binary signals.
3. State and explain the Duality principle with example.
4. Given the Boolean function $F = xyz + xyz + wxy + wxy + wxy$ i. Obtain the truth table of the function ii. Draw the logic diagram using the original Boolean expression iii. Simplify the function to a minimum number of literals using Booleanalgebra.
5. Implement the following Boolean function using AND, OR and inverter gates. $F = xy + x\ y + y\ z$.
6. Using the rules of boolean algebra, simplify the expressions that follow to the fewest total number of literals i. $f = AB + ABC + ACD$ ii. $f = B + AD + BC + [B+A(C+D)]1$
7. Simplify the following Boolean expression to a minimum number of literals.
   i. $F = (B\ C + A\ D)(A\ B + C\ D)$ ii. $F = WYZ + XY + X\ Z + YZ$
8. Express the following function in sum of minterms and product of maxterms. $F(A, B, C, D) = B\ D + A\ D + BD$

UNIT - III

1. Implement the following Boolean function with NAND gates $F(x,y,z) = \_\ (1,2,3,4,5,7)$.
2. Simplify the following Boolean function using four-variable map. $F(w, x, y, z) = \_\ (1, 3, 7, 11, 15) + d(0, 2, 5)$.
3. Find all the prime implicatiants for the following Boolean functions and determine which are essential.
   $F(A,B,C,D) = \_(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$
4. (a) Sum of product and (b) Product of sum expressions for the function given below $F(A, B, C, D) = \_(0, 1, 2, 5, 8, 9, 10)$

UNIT - IV

1. Implement a Boolean function $F(x, y, z) = \_\ (2, 4, 6)$ with a Multiplexer.
2. Explain about Tri - State gates in digital systems.

3. What is meant by encoder?
4. Design a 4 - input priority encoder.
5. Explain carry propagation in parallel adder with a neat diagram.
6. What is a decoder? Construct a 4×16 decoder with two 3×8 decoders.
7. Design a code converter that converts BCD to excess - 3 code.

UNIT – V

1. Design a D-type positive edge triggered flip flop.Also show the operation of the sequential circuit when CP = 1.
2. What is a flip flop.Design basic flip flop circuit with NAND gates.
3. Design a 4-bit register with parallel load using D flip flops
4. A sequential circuit has four flip flops A, B, C, D and an input x. State equations are as follows $A(t+1) = (CD1 + C1D)x + (CD + C1D1)x1$
   $B(t+1) = A$
   $C(t+1) = B$
   $D(t+1) = C$
5. Obtain the sequence of states when x=1, starting from state ABCD=0001and when x=0, starting from state ABCD=0001.Also draw the state diagram.
6. Design a clocked JK flip flop.
7. Define a latch and a flip flop. Mention the similarities and differences between them
8. Define the following terms related to filp-flops. set-up time hold time propagation delay preset and clear.
9. Distinguish between combinational logic and sequential logic.
10. Draw the circuit diagram of clocked D- flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.
11. A Sequential circuit with two D flip-flops A and B, two inputs x and y and one output z is specified by the following next-state and output equation. $A(t + 1) = xy + xA$ $z = B$ $B(t + 1) = xB + xA$
    i)Draw the logic diagram of the circuit.   ii)List the state table for the sequential circuit.   iii)Draw the corresponding state diagram.

UNIT – VI

1. What is a shift register. Draw the block diagram and timing diagram of a shift register that shows the serial transfer of information from register A to register B.
2. Define a ripple counter. Design a BCD ripple counter
3. Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4,5 using D- flip flops.
4. Distinguish between synchronous and asynchronous counters.
5. Write the HDL structural description of the 4- bit binary counter with parallel load.
6. Design a 4-bit ring counter using D- flip flops and draw the circuit diagram and timing diagrams.
7. Draw and explain 4-bit universal shift register.
8. Explain different types of shift registers.
9. Design a 4-bit ring counter using T- flip flops and draw the circuit diagram and timing diagrams.
10. Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram.
11. Design a 4-bit Johnson counter using T- flip flops and draw the circuit diagram and timing diagrams
12. Design a modulo -3 up/down synchronous counter using T- flip flops and draw the circuit diagram.
13. Write about the HDL behavioral description of a 4-bit shift register

UNIT – VII

1. A combinational circuit is defined by the functions
2. $F1(A,B,C) = \Sigma(3, 5, 6, 7)$,$F2(A,B,C) = \Sigma(0, 2, 4, 7)$ Explain in detail sequential programmable devices Implement the circuit with a PLA having 3 inputs , four product terms and two outputs
3. Explain in detail hazards in combinational networks.
4. Explain: a) Sequential programmable devices b) RAM and ROM

5. Give the HDL code for a memory read, write operations if the memory size is 64 words of 4 bits each. Also explain the code.
6. Tabulate the PLA programming table for the four Boolean functions: A(x,y,z) = _ (1,2,4,6)
   B(x,y,z) = _ (0,1,6,7)
   C(x,y,z) = _ (2,6)
   D(x,y,z) = _ (1,2,3,5,7)
7. Minimize the number of product terms and also show the internal logic in the PLA structure.
8. Draw and explain the block diagram of PAL.
9. Implement the following Boolean functions using PAL. w(A,B,C,D) = _ m (0,2,6,7,8,9,12,13)   x (A,B,C,D) = _m (0,2,6,7,8,9,12,13,14)   y (A,B,C,D) = _ m (2,3,8,9,10,12,13)   z (A,B,C,D) = _ m(1,3,4,6,9,12,14).
10. Explain the construction of a basic memory cell and also explain with diagram the construction of a 4 * 4 RAM
11. Given a 32*8 ROM chip with an enable input, show the external connections
12. Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform
13. List the PAL programming table and draw the PAL structure for the BCD-toexcess-3-code converter.
14. Explain about error detection and correction with example.

UNIT – VIII

1. Explain: a)Hazards in combinational networks.
   i. b) HDL for registers and counters
2. Explain: a) race-free state assignment hazards. i. b) PLA
3. Reduce the number of states in the state table listed below. Use an implication table Present state Next state Output
   x=0 x=1 x=0 x=1
   a f b 0 0
   b d c 0 0
   c f e 0 0
   d g a 0 0
   e d c 0 0
   f f b 1 1
   g g h 0 1
   h g a 1 0
4. Give the implementation procedure for a SR Latch using NOR gates.
5. Implement the circuit defined above with a NOR SR latch. Repeat with a NAND SR latch.
6. Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.
7. Explain the operation and use of De bounce circuit.
8. Explain the difference between asynchronous and synchronous sequential circuits.
   a. Define fundamental-mode operation.
   b. Explain the difference between stable and unstable states.
   c. What is the difference between an internal state and a total state.
9. Explain critical and non critical races with the help of example
10. Write about Hazards in sequential circuits.