VALLIAMMAI ENGINEERING COLLEGE

DEPARTMENT OF ELECTRICAL END ELECTRONICS ENGINEERING

EE6301 DIGITAL LOGIC CIRCUIT

YEAR/SEMESTER:II/III ACADEMIC YEAR:2014-2015

UNIT 1
NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES
PART A

1. Briefly explain the stream lined method of converting binary to decimal number with example.
2. Give the Gray code for the binary number $(111)_2$.
3. When can RTL be used to represent digital systems?
4. State the important characteristics of TTL family.
5. What weight does the digit 5 have in each of the following decimal number?(a)1530 (b)1.059(c)3258(d)567.
6. Convert following hexadecimal number to decimal number.(a)$F28_{16}$ (b) $BC2_{16}$
7. Convert following decimal number to hexadecimal.(a)1259(b)5768.
8. Convert (a)1001001110101101_2 (b)10010001011.00101110_2 to hexadecimal.
9. Convert 3576_8 to hexadecimal.
10. Classify the logic family by operation
11. List the advantages of ECL as compared to TTL logic family.
12. Classify the basic families that belong to the bipolar families and to the MOS families.

    Ans: logic families:
    - Bipolar
    - MOS

    Bipolar:
    - TTL
    - DTL
    - RTL
    - ECL

    MOS:
    - CMOS
    - NMOS
    - PMOS

13. Which is faster TTL or ECL? Which requires more power to operate?
14. Define noise margin.
15. Define Fan-out?
16. Define power dissipation?
17. What is propagation delay?
18. Define fan in?
19. Mention the classification of saturated bipolar logic families.
20. What are the types of TTL logic?
21. Express a 15 bit hamming code in general.

PART B

1. Discuss about TTL parameters.

2. Draw and explain the circuit diagram of CMOS NOR gate.
3. Name and explain the characteristics of TTL family.
4. Explain the characteristics and implementation of the following digital logic families. (a) CMOS (b) ECL (c) TTL
5. Describe the concept working and applications of the following memories: (a)PLD(b)FPGA(c)EPROM
6. Explain the classifications of binary codes.
7. Explain about error detection and correction codes

UNIT 2
COMBINATIONAL CIRCUITS
PART A

1. Why is MUX called as data selector?
2. Which gates are called as the universal gates?
3. Define binary logic?
4. What are the basic digital logic gates?
5. What is a Logic gate?
6. Define combinational logic.
7. Explain the design procedure for combinational circuits.
8. Define Half adder and full adder.
9. Define Decoder?
10. What is binary decoder?
11. Define Encoder?
12. What is priority Encoder?
13. Define multiplexer?
14. What do you mean by comparator?

PART B

1. Obtain the minimum SOP using QUINE- McCLUSKY method and verify using K-map $F=m_0+m_2+m_4+m_8+m_9+m_{10}+m_{11}+m_{12}+m_{13}$
2. Reduce the following using tabulation method.
3. $F=m_2+m_3+m_4+m_6+m_7+m_9+m_{11}+m_{13}$.
4. Reduce the Boolean function using k-map technique and implement using gates f (w, x, y, z)= Σm (0,1,4,8,9,10) which has the don't cares condition d (w, x, y, z)= Σm (2,11).
5. (a)Design an 8421 to gray code converter. (b)Implement the Boolean function using 8:1 mux F (A, B, C, D) =A'BD'+ACD+B'CD+A'C'D.
6. Design A Full Adder And A Full Subtractor.
7. A combinational circuit is defined by the following three Boolean functions F1 = x'y'z'+xz F2= xy'z'+x'y F3= x'y'z+xy. Design the circuit with a decoder and external gates.
8. Simplify the following Boolean function by using Tabulation method F (w, x, y, z) =∑m (0, 1, 2, 8, 10, 11, 14, 15)
9. Simplify the following Boolean functions by using K'Map in SOP & POS.

F (w, x, y, z) = ∑m (1, 3, 4, 6, 9, 11, 12, 14)

10. (a) Design a 2 bit magnitude comparator. (b) Explain the operation of 4 to 10 decoder.
11. Design a 4-bit binary to excess-3 converter using the unused combinations of the code as don't care conditions. Represent the converter using logic diagram.

UNIT 3
SYNCHRONOUS SEQUENTIAL CIRCUITS
PART A

1. What are the classification of sequential circuits?
2. Define Flip flop.
3. What are the different types of flip-flop?
4. What is the operation of D flip-flop?
5. What is the operation of JK flip-flop?
6. What is the operation of T flip-flop?
7. Define race around condition.
8. What is edge-triggered flip-flop?
9. What is a master-slave flip-flop?
10. Define rise time.
11. Define fall time.
12. Define skew and clock skew.
13. Define setup time.
14. Define hold time.
15. Define propagation delay.
16. Define registers.
17. Define sequential circuit?
18. Give the comparison between combinational circuits and sequential circuits.
19. What do you mean by present state?
20. What do you mean by next state?
21. State the types of sequential circuits?
22. Define synchronous sequential circuit

PART B

1. A sequential circuit has 2D ff's A and B an input x and output y is specified by the following next state and output equations.
    a. A (t+1)= Ax + Bx
    b. B (t+1)= A'x
    c. Y= (A+B) x'

    (i) Draw the logic diagram of the circuit.
    (ii) Derive the state table.
    (iii) Derive the state diagram.
2. Design a mod-10 synchronous counter using Jk ff. write excitation table and state table.
3. a) Write the excitation tables of SR, JK, D, and T Flip flops (b) Realize D and T flip flops using Jk flip flops
4. Design a sequential circuit using JK flip-flop for the following state table [use state diagram]

Present state	Next state		Output	
AB	X=0	X=1	X=0	X=1
00	00	11	1	0
01	01	11	1	1
10	01	00	1	0
11	11	10	0	0

5. Design a counter with the following repeated binary sequence:0, 1, 2, 3, 4, 5, 6.use JK Flip-flop.
6. Design a 3 bit synchronous gray code counter using flip flop.
7. Draw and explain the block diagram of Mealy circuit.
8. Using positive edge triggering SR flip-flops design a counter which counts in the following sequence: 000,111,110,101,100,011,010,001,000,…

UNIT 4
ASYNCHRONOUS SEQUENTIAL CIRCUITS & PROGRAMMABLE LOGIC DEVICES
PARTA

1. Define Asynchronous sequential circuit?
2. Give the comparison between synchronous & Asynchronous sequential circuits?
3. The following wave forms are applied to the inputs of SR latch. Determine the Q waveform Assume initially Q = 1 4.
4. What is race around condition?
5. Give the comparison between synchronous & Asynchronous counters.
6. The t pd for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter
7. What are secondary variables?
8. What are excitation variables?
9. What is fundamental mode sequential circuit?
10. What are pulse mode circuit?
11. What are the significance of state assignment?
12. When do race condition occur?
13. What is non critical race?
14. What is critical race?
15. When does a cycle occur?
16. What are the different techniques used in state assignment?
17. What are the steps for the design of asynchronous sequential circuit?
18. What is hazard?
19. What is static 1 hazard?
20. What is static 0 hazard?
21. What is dynamic hazard?
22. What is the cause for essential hazards?
23. What is flow table?
24. . What is primitive flow chart?
25. What is combinational circuit?
26. Define merger graph.
27. Define closed covering.

28. Define state table.
29. Define total state
30. What are the steps for the design of asynchronous sequential circuit?
31. Define primitive flow table.
32. What are the types of asynchronous circuits?
33. Give the comparison between state Assignment Synchronous circuit and state assignment asynchronous circuit.
34. What are races?
35. Define non critical race.
36. Define critical race?
37. What is a cycle?
38. Write a short note on fundamental mode asynchronous circuit.
39. Write a short note on pulse mode circuit.
40. Define secondary variables.
41. Define flow table in asynchronous sequential circuit.
42. What is fundamental mode.
43. Write short note on shared row state assignment.
44. Write short note on one hot state assignment.
45. A pulse mode asynchronous machine has two inputs. If produces an output whenever two consecutive pulses occur on one input line only. The output remains at 1 until a pulse has occurred on the other input line. Write down the state table for the machine.
46. What is programmable logic array? How it differs from ROM?
47. Explain EPROM.
48. Give the classification of PLD's.
49. Define PROM.
50. Define PLA
51. Define PAL
52. Why was PAL developed ?
53. Why the input variables to a PAL are buffered
54. What does PAL 10L8 specify ?
55. Give the comparison between PROM and PLA.

PART B

1. Design an asynchronous sequential circuit that has 2 inputs x2 and x1, and one output z. the output is to remain 0 as long as an X1 is 0. The first change in x2 that occurs while x1 is 1 will cause z to be 1. Z is to remain 1 until x1 returns to 0. Construct a state diagram and flow table. Determine the output equations.
2. Design a circuit with inputs A and B to give an output z=1 when AB=11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included
3. Obtain the primitive flow table for an asynchronous circuit that has 2 input's x, y and output z. an output z=1, is to occur only during the input state xy=01 and then if and only if the input state xy=01 is preceded by the input sequence xy=01, 00, 10, 00, 10, 00
4. Design a circuit with input a and b to give an output z=1 when AB =11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and

output map in which transient state is included.

5. Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T = 1 & c moves from 1 to 0. Otherwise the output is 0.
6. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input
7. a. Explain the difference between synchronous and asynchronous sequential circuits. b. Derive the transition table for the asynchronous sequential circuit shown below. Determine the sequence of internal states Y1Y2 for the following sequence of inputs x1x2 : 00,10,11,01,11,10,00.
8. Derive the transition table and logic diagram for an asynchronous sequential circuit with the help of the following flow table.
9. a) Explain in detail about PLA with a specific example. b) Explain with neat diagrams RAM architecture
10. Implement the following function using PLA.
    a. A (x, y, z) = ∑m (1, 2, 4, 6)
    b. B (x, y, z) = ∑m (0, 1, 6, 7)
    c. C (x, y, z) = ∑m (2, 6)
11. Implement the following function using PAL.
    a. W (A, B, C, D) = ∑m (2, 12, 13)
    b. X (A, B, C, D) = ∑m (7, 8, 9, 10, 11, 12, 13, 14, 15)
    c. Y (A, B, C, D) = ∑m (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)
    d. Z (A, B, C, D) = ∑m (1, 2, 8, 12, 13)
12. Discuss on the concept of working and applications of following memories.
    i. ROM
    ii. EPROM
    iii. PLA.
13. i) A combinational circuit is defined by the functions.
    a. F1 (a, b, c) = ∑ m (3, 5, 6, 7)
    b. F2 (a, b, c) = ∑ m (0, 2, 4, 7) implement the circuit with a PLA.

    ii) Write short notes on semiconductor memories

UNIT 5
VHDL
PART A

1. What do the acronyms VHDL and VHLSI stand for?
2. What are the different types of modeling VHDL?
3. What is packages and what is the use of these packages
4. What is variable class ,give example for variable
5. Name two subprograms and give the difference between these two.
6. What is subprogram Overloading
7. Write the VHDL coding for a sequential statement (d-flipflop)
8. What are the different kinds of the test bench?
9. What is Moore FSM
10. Write the testbench for and gate

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PART B

1. Write a HDL code for state machine to BCD to ex–3 codes Converter.
2. Write a behavioral VHDL description of an S-R latch using a process
3. Write a HDL code for 8:1 MUX using behavioral model
4. Write the HDL description of the circuit specified by the Following Boolean equations
    a. S = xy '+ x' y
    b. C =xy
5. (I) Write an HDL data flow description of a 4 bit adder subtractor of Unsigned numbers use the conditional operator (II) Write the HDL gate level description of the priority encoder
6. (I) Write VHDL code for a full sub tractor using logic Equation
   (II) Write a VHDL description of an S-R latch using a process